2x QSFP28 FMC Datasheet

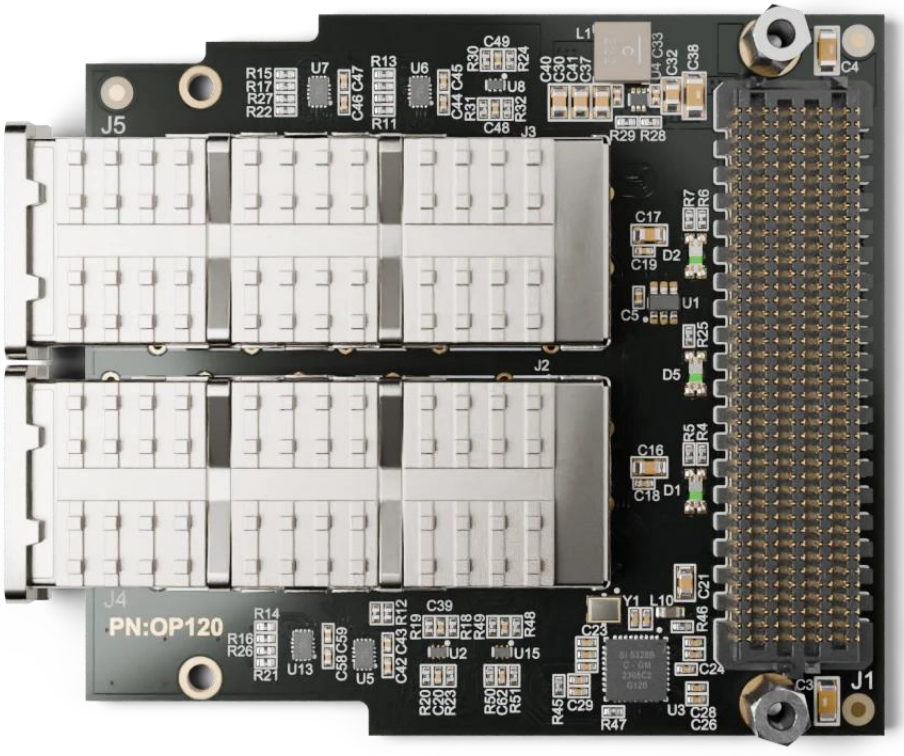
Part number: OP120

Overview

Description

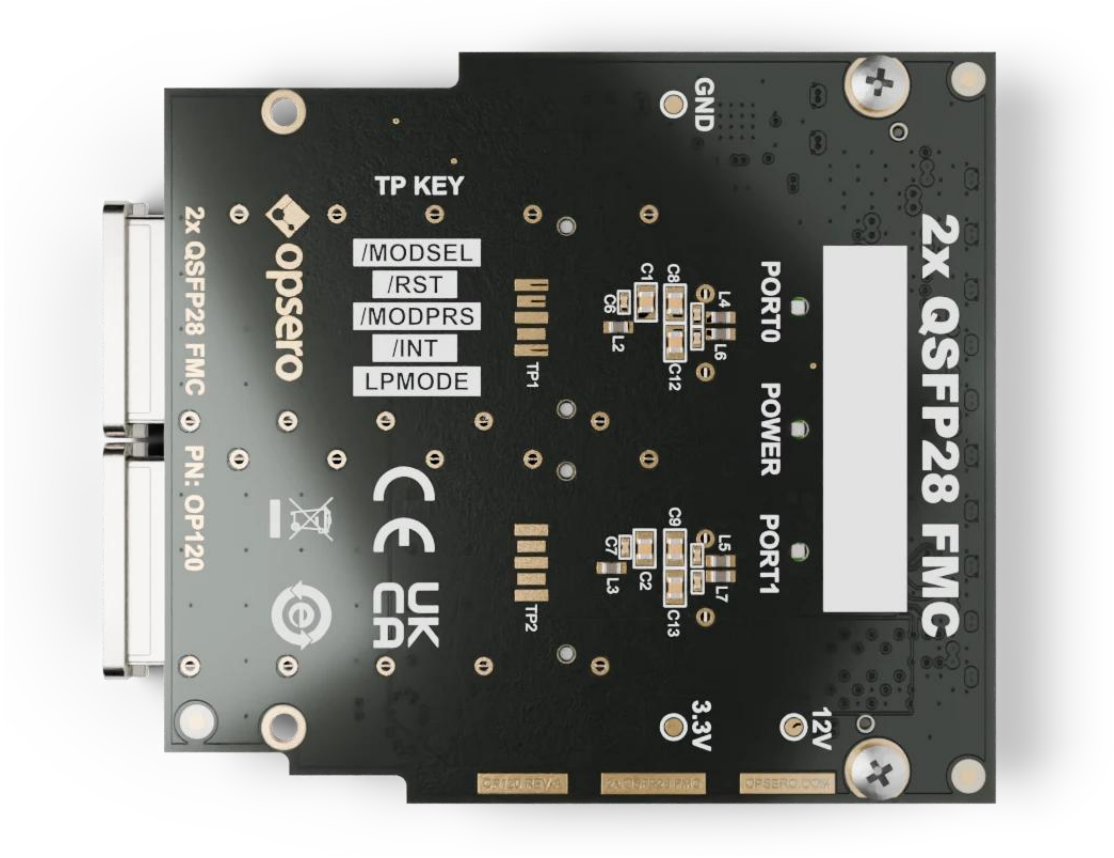
The 2x QSFP28 FMC is an add-on expansion board (FPGA Mezzanine Card) for FPGA and SoC-based development boards. It has two QSFP28 module slots, allowing the connection of up to two QSFP28, QSFP+ or QSFP modules to the carrier development board. Each QSFP28 port provides four lanes of up to 25 Gbps each, for an aggregate bandwidth of up to 100 Gbps per port. The mezzanine card features a jitter-attenuating clock multiplier, supporting Synchronous Ethernet applications, and uses level translators to support a wide range of FPGA I/O voltages from 1.2VDC to 3.3VDC.

Top view



2x QSFP28 FMC top

Bottom view



2x QSFP28 FMC bottom

Features

- 2x QSFP28 slots compatible with QSFP, QSFP+ and QSFP28 modules
- Each port provides 4x lanes of up to 25 Gbps (100 Gbps aggregate per port)
- Jitter-attenuating clock multiplier with support for recovered clock and SyncE applications
- Supports a wide range of I/O voltages (VADJ): 1.2V-3.3V
- High pin count FMC connector
- FMC pinout conforms to VITA 57.1 FMC Standard
- Testpoints to aid debugging
- Example designs with sources for several development boards

- Standalone and PetaLinux example designs

Ordering

The 2x QSFP28 FMC can be ordered from the vendors listed below. The links under the part number column will take you to the corresponding order page.

Vendor	Part name	Part number
Opsero	2x QSFP28 FMC	OP120
Digi-Key	2x QSFP28 FMC	OP120

Included with the 2x QSFP28 FMC are 2x machine screws for fixing the mezzanine card to the carrier board.

Pin Configuration

Pinout table

The 2x QSFP28 FMC has a high pin count FPGA Mezzanine Card (FMC) connector, providing the connections to the FPGA on the development board. The following table defines the pinout of the FMC connector and describes each pin's purpose on this mezzanine card.

Pin	Pin name	Net	Description
A1	GND	GND	Ground
A2	DP1_M2C_P	DP1_M2C_P	Port 0 QSFP28 RX lane 1 positive
A3	DP1_M2C_N	DP1_M2C_N	Port 0 QSFP28 RX lane 1 negative
A4	GND	GND	Ground
A5	GND	GND	Ground

A6	DP2_M2C_P	DP2_M2C_P	Port 0 QSFP28 RX lane 2 positive
A7	DP2_M2C_N	DP2_M2C_N	Port 0 QSFP28 RX lane 2 negative
A8	GND	GND	Ground
A9	GND	GND	Ground
A10	DP3_M2C_P	DP3_M2C_P	Port 0 QSFP28 RX lane 3 positive
A11	DP3_M2C_N	DP3_M2C_N	Port 0 QSFP28 RX lane 3 negative
A12	GND	GND	Ground
A13	GND	GND	Ground
A14	DP4_M2C_P	DP4_M2C_P	Port 1 QSFP28 RX lane 0 positive
A15	DP4_M2C_N	DP4_M2C_N	Port 1 QSFP28 RX lane 0 negative
A16	GND	GND	Ground
A17	GND	GND	Ground
A18	DP5_M2C_P	DP5_M2C_P	Port 1 QSFP28 RX lane 1 positive
A19	DP5_M2C_N	DP5_M2C_N	Port 1 QSFP28 RX lane 1 negative
A20	GND	GND	Ground
A21	GND	GND	Ground

A22	DP1_C2M_P	DP1_C2M_P	Port 0 QSFP28 TX lane 1 positive
A23	DP1_C2M_N	DP1_C2M_N	Port 0 QSFP28 TX lane 1 negative
A24	GND	GND	Ground
A25	GND	GND	Ground
A26	DP2_C2M_P	DP2_C2M_P	Port 0 QSFP28 TX lane 2 positive
A27	DP2_C2M_N	DP2_C2M_N	Port 0 QSFP28 TX lane 2 negative
A28	GND	GND	Ground
A29	GND	GND	Ground
A30	DP3_C2M_P	DP3_C2M_P	Port 0 QSFP28 TX lane 3 positive
A31	DP3_C2M_N	DP3_C2M_N	Port 0 QSFP28 TX lane 3 negative
A32	GND	GND	Ground
A33	GND	GND	Ground
A34	DP4_C2M_P	DP4_C2M_P	Port 1 QSFP28 TX lane 0 positive
A35	DP4_C2M_N	DP4_C2M_N	Port 1 QSFP28 TX lane 0 negative
A36	GND	GND	Ground
A37	GND	GND	Ground

A38	DP5_C2M_P	DP5_C2M_P	Port 1 QSFP28 TX lane 1 positive
A39	DP5_C2M_N	DP5_C2M_N	Port 1 QSFP28 TX lane 1 negative
A40	GND	GND	Ground
B1	CLK_DIR	N/C	Not connected
B2	GND	GND	Ground
B3	GND	GND	Ground
B4	DP9_M2C_P	N/C	Not connected
B5	DP9_M2C_N	N/C	Not connected
B6	GND	GND	Ground
B7	GND	GND	Ground
B8	DP8_M2C_P	N/C	Not connected
B9	DP8_M2C_N	N/C	Not connected
B10	GND	GND	Ground
B11	GND	GND	Ground
B12	DP7_M2C_P	DP7_M2C_P	Port 1 QSFP28 RX lane 3 positive
B13	DP7_M2C_N	DP7_M2C_N	Port 1 QSFP28 RX lane 3 negative
B14	GND	GND	Ground
B15	GND	GND	Ground
B16	DP6_M2C_P	DP6_M2C_P	Port 1 QSFP28 RX lane 2 positive

B17	DP6_M2C_N	DP6_M2C_N	Port 1 QSFP28 RX lane 2 negative
B18	GND	GND	Ground
B19	GND	GND	Ground
B20	GBTCLK1_M2C_P	GBTCLK1_M2C_P	Clock oscillator Si5328 CLKOUT2+ output
B21	GBTCLK1_M2C_N	GBTCLK1_M2C_N	Clock oscillator Si5328 CLKOUT2- output
B22	GND	GND	Ground
B23	GND	GND	Ground
B24	DP9_C2M_P	N/C	Not connected
B25	DP9_C2M_N	N/C	Not connected
B26	GND	GND	Ground
B27	GND	GND	Ground
B28	DP8_C2M_P	N/C	Not connected
B29	DP8_C2M_N	N/C	Not connected
B30	GND	GND	Ground
B31	GND	GND	Ground
B32	DP7_C2M_P	DP7_C2M_P	Port 1 QSFP28 TX lane 3 positive
B33	DP7_C2M_N	DP7_C2M_N	Port 1 QSFP28 TX lane 3 negative
B34	GND	GND	Ground

B35	GND	GND	Ground
B36	DP6_C2M_P	DP6_C2M_P	Port 1 QSFP28 TX lane 2 positive
B37	DP6_C2M_N	DP6_C2M_N	Port 1 QSFP28 TX lane 2 negative
B38	GND	GND	Ground
B39	GND	GND	Ground
B40	RES0	N/C	Not connected
C1	GND	GND	Ground
C2	DP0_C2M_P	DP0_C2M_P	Port 0 QSFP28 TX lane 0 positive
C3	DP0_C2M_N	DP0_C2M_N	Port 0 QSFP28 TX lane 0 negative
C4	GND	GND	Ground
C5	GND	GND	Ground
C6	DP0_M2C_P	DP0_M2C_P	Port 0 QSFP28 RX lane 0 positive
C7	DP0_M2C_N	DP0_M2C_N	Port 0 QSFP28 RX lane 0 negative
C8	GND	GND	Ground
C9	GND	GND	Ground
C10	LA06_P	CLK_LOS_ALARM_T	Clock loss alarm from Si5328
C11	LA06_N	N/C	Not connected
C12	GND	GND	Ground

C13	GND	GND	Ground
C14	LA10_P	N/C	Not connected
C15	LA10_N	N/C	Not connected
C16	GND	GND	Ground
C17	GND	GND	Ground
C18	LA14_P	N/C	Not connected
C19	LA14_N	N/C	Not connected
C20	GND	GND	Ground
C21	GND	GND	Ground
C22	LA18_P_CC	N/C	Not connected
C23	LA18_N_CC	N/C	Not connected
C24	GND	GND	Ground
C25	GND	GND	Ground
C26	LA27_P	N/C	Not connected
C27	LA27_N	N/C	Not connected
C28	GND	GND	Ground
C29	GND	GND	Ground
C30	SCL	I2C_SCL	I2C Clock
C31	SDA	I2C_SDA	I2C Data (bidirectional)
C32	GND	GND	Ground
C33	GND	GND	Ground
C34	GA0	GA0	EEPROM Address Bit 1 (A1)

C35	12P0V_1	12V0	12VDC
C36	GND	GND	Ground
C37	12P0V_2	12V0	12VDC
C38	GND	GND	Ground
C39	3P3V_1	3V3	Not connected
C40	GND	GND	Ground
D1	PG_C2M	PG	Power Good (Driven by carrier)
D2	GND	GND	Ground
D3	GND	GND	Ground
D4	GBTCLK0_M2C_P	GBTCLK0_M2C_P	Clock oscillator Si5328 CLKOUT1+ output
D5	GBTCLK0_M2C_N	GBTCLK0_M2C_N	Clock oscillator Si5328 CLKOUT1- output
D6	GND	GND	Ground
D7	GND	GND	Ground
D8	LA01_P_CC	N/C	Not connected
D9	LA01_N_CC	N/C	Not connected
D10	GND	GND	Ground
D11	LA05_P	QSFP1_MODPRSL_T	Port 1 QSFP28 Module Present (active low)

D12	LA05_N	QSFP1_INTL_T	Port 1 QSFP28 Interrupt (active low)
D13	GND	GND	Ground
D14	LA09_P	N/C	Not connected
D15	LA09_N	N/C	Not connected
D16	GND	GND	Ground
D17	LA13_P	N/C	Not connected
D18	LA13_N	N/C	Not connected
D19	GND	GND	Ground
D20	LA17_P_CC	QSFP1_I2C_SCL_T	Port 1 QSFP28 I2C Clock
D21	LA17_N_CC	QSFP1_I2C_SDA_T	Port 1 QSFP28 I2C Data (bidirectional)
D22	GND	GND	Ground
D23	LA23_P	N/C	Not connected
D24	LA23_N	N/C	Not connected
D25	GND	GND	Ground
D26	LA26_P	N/C	Not connected
D27	LA26_N	N/C	Not connected
D28	GND	GND	Ground
D29	TCK	N/C	Not connected
D30	TDI	TDI	Connects to TDO to close JTAG chain

D31	TDO	TDO	Connects to TDI to close JTAG chain
D32	3P3VAUX	3V3AUX	3.3VDC Power supply for EEPROM
D33	TMS	N/C	Not connected
D34	TRST_L	N/C	Not connected
D35	GA1	GA1	EEPROM Address Bit 0 (A0)
D36	3P3V_2	3V3	3.3VDC main FMC power supply
D37	GND	GND	Ground
D38	3P3V_3	3V3	3.3VDC main FMC power supply
D39	GND	GND	Ground
D40	3P3V_4	3V3	3.3VDC main FMC power supply
E1	GND	GND	Ground
E2	HA01_P_CC	N/C	Not connected
E3	HA01_N_CC	N/C	Not connected
E4	GND	GND	Ground
E5	GND	GND	Ground
E6	HA05_P	N/C	Not connected
E7	HA05_P	N/C	Not connected
E8	GND	GND	Ground
E9	HA09_P	N/C	Not connected

E10	HA09_P	N/C	Not connected
E11	GND	GND	Ground
E12	HA13_P	N/C	Not connected
E13	HA13_P	N/C	Not connected
E14	GND	GND	Ground
E15	HA16_P	N/C	Not connected
E16	HA16_P	N/C	Not connected
E17	GND	GND	Ground
E18	HA20_P	N/C	Not connected
E19	HA20_P	N/C	Not connected
E20	GND	GND	Ground
E21	HB03_P	N/C	Not connected
E22	HB03_P	N/C	Not connected
E23	GND	GND	Ground
E24	HB05_P	N/C	Not connected
E25	HB05_P	N/C	Not connected
E26	GND	GND	Ground
E27	HB09_P	N/C	Not connected
E28	HB09_P	N/C	Not connected
E29	GND	GND	Ground
E30	HB13_P	N/C	Not connected
E31	HB13_P	N/C	Not connected
E32	GND	GND	Ground

E33	HB19_P	N/C	Not connected
E34	HB19_P	N/C	Not connected
E35	GND	GND	Ground
E36	HB21_P	N/C	Not connected
E37	HB21_P	N/C	Not connected
E38	GND	GND	Ground
E39	VADJ_1	N/C	Adjustable IO power supply voltage
E40	GND	GND	Ground
F1	PG_M2C	N/C	Not connected
F2	GND	GND	Ground
F3	GND	GND	Ground
F4	HA00_P_CC	N/C	Not connected
F5	HA00_P_CC	N/C	Not connected
F6	GND	GND	Ground
F7	HA04_P	N/C	Not connected
F8	HA04_P	N/C	Not connected
F9	GND	GND	Ground
F10	HA08_P	N/C	Not connected
F11	HA08_P	N/C	Not connected
F12	GND	GND	Ground
F13	HA12_P	N/C	Not connected
F14	HA12_P	N/C	Not connected

F15	GND	GND	Ground
F16	HA15_P	N/C	Not connected
F17	HA15_P	N/C	Not connected
F18	GND	GND	Ground
F19	HA19_P	N/C	Not connected
F20	HA19_P	N/C	Not connected
F21	GND	GND	Ground
F22	HB02_P	N/C	Not connected
F23	HB02_P	N/C	Not connected
F24	GND	GND	Ground
F25	HB04_P	N/C	Not connected
F26	HB04_P	N/C	Not connected
F27	GND	GND	Ground
F28	HB08_P	N/C	Not connected
F29	HB08_P	N/C	Not connected
F30	GND	GND	Ground
F31	HB12_P	N/C	Not connected
F32	HB12_P	N/C	Not connected
F33	GND	GND	Ground
F34	HB16_P	N/C	Not connected
F35	HB16_P	N/C	Not connected
F36	GND	GND	Ground
F37	HB20_P	N/C	Not connected

F38	HB20_P	N/C	Not connected
F39	GND	GND	Ground
F40	VADJ_2	N/C	Adjustable IO power supply voltage
J1	GND	GND	Ground
J2	CLK3_BIDIR_P	N/C	Not connected
J3	CLK3_BIDIR_P	N/C	Not connected
J4	GND	GND	Ground
J5	GND	GND	Ground
J6	HA03_P	N/C	Not connected
J7	HA03_P	N/C	Not connected
J8	GND	GND	Ground
J9	HA07_P	N/C	Not connected
J10	HA07_P	N/C	Not connected
J11	GND	GND	Ground
J12	HA11_P	N/C	Not connected
J13	HA11_P	N/C	Not connected
J14	GND	GND	Ground
J15	HA14_P	N/C	Not connected
J16	HA14_P	N/C	Not connected
J17	GND	GND	Ground
J18	HA18_P	N/C	Not connected
J19	HA18_P	N/C	Not connected

J20	GND	GND	Ground
J21	HA22_P	N/C	Not connected
J22	HA22_P	N/C	Not connected
J23	GND	GND	Ground
J24	HB01_P	N/C	Not connected
J25	HB01_P	N/C	Not connected
J26	GND	GND	Ground
J27	HB07_P	N/C	Not connected
J28	HB07_P	N/C	Not connected
J29	GND	GND	Ground
J30	HB11_P	N/C	Not connected
J31	HB11_P	N/C	Not connected
J32	GND	GND	Ground
J33	HB15_P	N/C	Not connected
J34	HB15_P	N/C	Not connected
J35	GND	GND	Ground
J36	HB18_P	N/C	Not connected
J37	HB18_P	N/C	Not connected
J38	GND	GND	Ground
J39	VIO_B_M2C_1	N/C	Not connected
J40	GND	GND	Ground
K1	VREF_B_M2C	N/C	Not connected
K2	GND	GND	Ground

K3	GND	GND	Ground
K4	CLK2_BIDIR_P	N/C	Not connected
K5	CLK2_BIDIR_P	N/C	Not connected
K6	GND	GND	Ground
K7	HA02_P	N/C	Not connected
K8	HA02_P	N/C	Not connected
K9	GND	GND	Ground
K10	HA06_P	N/C	Not connected
K11	HA06_P	N/C	Not connected
K12	GND	GND	Ground
K13	HA10_P	N/C	Not connected
K14	HA10_P	N/C	Not connected
K15	GND	GND	Ground
K16	HA17_P_CC	N/C	Not connected
K17	HA17_P_CC	N/C	Not connected
K18	GND	GND	Ground
K19	HA21_P	N/C	Not connected
K20	HA21_P	N/C	Not connected
K21	GND	GND	Ground
K22	HA23_P	N/C	Not connected
K23	HA23_P	N/C	Not connected
K24	GND	GND	Ground
K25	HB00_P_CC	N/C	Not connected

K26	HB00_P_CC	N/C	Not connected
K27	GND	GND	Ground
K28	HB06_P_CC	N/C	Not connected
K29	HB06_P_CC	N/C	Not connected
K30	GND	GND	Ground
K31	HB10_P	N/C	Not connected
K32	HB10_P	N/C	Not connected
K33	GND	GND	Ground
K34	HB14_P	N/C	Not connected
K35	HB14_P	N/C	Not connected
K36	GND	GND	Ground
K37	HB17_P_CC	N/C	Not connected
K38	HB17_P_CC	N/C	Not connected
K39	GND	GND	Ground
K40	VIO_B_M2C_2	N/C	Not connected
G1	GND	GND	Ground
G2	CLK1_M2C_P	N/C	Not connected
G3	CLK1_M2C_N	N/C	Not connected
G4	GND	GND	Ground
G5	GND	GND	Ground
G6	LA00_P_CC	REC_CLK1_P	Recovered clock positive (LVDS, FPGA to Si5328)

G7	LA00_N_CC	REC_CLK1_N	Recovered clock negative (LVDS, FPGA to Si5328)
G8	GND	GND	Ground
G9	LA03_P	QSFP0_I2C_SCL_T	Port 0 QSFP28 I2C Clock
G10	LA03_N	QSFP0_I2C_SDA_T	Port 0 QSFP28 I2C Data (bidirectional)
G11	GND	GND	Ground
G12	LA08_P	QSFP1_GRN_LED_T	Port 1 QSFP28 User bicolor LED Green
G13	LA08_N	QSFP1_RED_LED_T	Port 1 QSFP28 User bicolor LED Red
G14	GND	GND	Ground
G15	LA12_P	QSFP0_MODPRSL_T	Port 0 QSFP28 Module Present (active low)
G16	LA12_N	QSFP0_INTL_T	Port 0 QSFP28 Interrupt (active low)
G17	GND	GND	Ground
G18	LA16_P	N/C	Not connected
G19	LA16_N	N/C	Not connected
G20	GND	GND	Ground
G21	LA20_P	N/C	Not connected
G22	LA20_N	N/C	Not connected

G23	GND	GND	Ground
G24	LA22_P	N/C	Not connected
G25	LA22_N	N/C	Not connected
G26	GND	GND	Ground
G27	LA25_P	N/C	Not connected
G28	LA25_N	N/C	Not connected
G29	GND	GND	Ground
G30	LA29_P	N/C	Not connected
G31	LA29_N	N/C	Not connected
G32	GND	GND	Ground
G33	LA31_P	N/C	Not connected
G34	LA31_N	N/C	Not connected
G35	GND	GND	Ground
G36	LA33_P	N/C	Not connected
G37	LA33_N	N/C	Not connected
G38	GND	GND	Ground
G39	VADJ_3	VADJ	Adjustable IO power supply voltage
G40	GND	GND	Ground
H1	VREF_A_M2C	N/C	Not connected
H2	PRSNT_M2C_L	GND	Ground
H3	GND	GND	Ground
H4	CLK0_M2C_P	N/C	Not connected

H5	CLK0_M2C_N	N/C	Not connected
H6	GND	GND	Ground
H7	LA02_P	CLK_I2C_SCL_T	Clock multiplier I2C bus clock SCL
H8	LA02_N	CLK_I2C_SDA_T	Clock multiplier I2C bus data SDA
H9	GND	GND	Ground
H10	LA04_P	QSFP0_MODSELL_T	Port 0 QSFP28 Module Select (active low)
H11	LA04_N	QSFP0_RESETL_T	Port 0 QSFP28 Reset (active low)
H12	GND	GND	Ground
H13	LA07_P	QSFP0_GRN_LED_T	Port 0 QSFP28 User bicolor LED Green
H14	LA07_N	QSFP0_RED_LED_T	Port 0 QSFP28 User bicolor LED Red
H15	GND	GND	Ground
H16	LA11_P	QSFP0_LPMODE_T	Port 0 QSFP28 Low Power Mode
H17	LA11_N	QSFP1_LPMODE_T	Port 1 QSFP28 Low Power Mode
H18	GND	GND	Ground
H19	LA15_P	QSFP1_MODSELL_T	Port 1 QSFP28 Module Select (active low)

H20	LA15_N	QSFP1_RESETL_T	Port 1 QSFP28 Reset (active low)
H21	GND	GND	Ground
H22	LA19_P	N/C	Not connected
H23	LA19_N	N/C	Not connected
H24	GND	GND	Ground
H25	LA21_P	N/C	Not connected
H26	LA21_N	N/C	Not connected
H27	GND	GND	Ground
H28	LA24_P	N/C	Not connected
H29	LA24_N	N/C	Not connected
H30	GND	GND	Ground
H31	LA28_P	N/C	Not connected
H32	LA28_N	N/C	Not connected
H33	GND	GND	Ground
H34	LA30_P	N/C	Not connected
H35	LA30_N	N/C	Not connected
H36	GND	GND	Ground
H37	LA32_P	N/C	Not connected
H38	LA32_N	N/C	Not connected
H39	GND	GND	Ground
H40	VADJ_4	VADJ	Adjustable IO power supply voltage

Specifications

Recommended Operating Conditions

SUPPLY VOLTAGE	MIN	TYP	MAX	UNIT
12 VDC	+11.4	+12	+12.6	V
3.3 VDC	+3.14	+3.3	+3.46	V
VADJ (1.2VDC)	+1.14	+1.2	+1.26	V
VADJ (1.5VDC)	+1.425	+1.5	+1.575	V
VADJ (1.8VDC)	+1.71	+1.8	+1.89	V
VADJ (2.5VDC)	+2.375	+2.5	+2.625	V
VADJ (3.3VDC)	+3.135	+3.3	+3.465	V

Notes:

- All VADJ pins must be supplied with the same voltage chosen from one of the following levels: +1.2VDC, +1.5VDC, +1.8VDC, +2.5VDC, +3.3VDC. Note that many carriers have a system controller that will make this choice for you.

Power Consumption

The power consumption of the 2x QSFP28 FMC will depend heavily on the QSFP28 modules being used and the load they are being put under. Power consumption measurements will be added to this section in the near future.

Thermal Information

We have not performed comprehensive thermal testing on the 2x QSFP28 FMC, however we recommend that it be operated under ambient temperatures between -40 and 85 degrees C. This advice is based on the recommended ambient operating temperatures of a basket of QSFP28 modules currently on the market. The active devices on the mezzanine card itself have operating ranges that match or exceed those of typical QSFP28 modules and are listed in the table below.

DEVICE	MIN	MAX	UNIT
TI, 3-16V 5A Buck Converter, TPS565247DRLR	-40	150	C
TI, I2C Level Translator, TCA9416DDFR	-40	125	C
Microchip, 2Kbit EEPROM, 34AA02T-I/OT	-40	85	C
Skyworks, SyncE Jitter-Attenuating Clock Multiplier, SI5328B-C-GM	-40	85	C
TI, Level Translator, SN74AVC4T245RSVR	-40	85	C
Abracon, 114.285MHz Crystal, ABM8-166-114.285MHZ-T2	-40	85	C

Components that are not listed in the table above (such as resistors, capacitors) are selected to have minimum operating temperature that is lower than -40 degrees C, and maximum operating temperature that is greater than 85 degrees C.

I2C (EEPROM) Timing

The serial EEPROM (part number Microchip, 2Kbit EEPROM, 34AA02T-I/OT) has a maximum operating clock frequency of 400 kHz (Fast-mode).

I2C (CLK, QSFP0/1) Timing

The three PL I2C buses pass through level translators (TCA9416) that support an I2C clock frequency up to 1MHz (Fast-mode Plus).

Device	Standard-mode 100kHz	Fast-mode 400kHz	Fast-mode Plus 1MHz
Level translator TCA9416	:white_check_mark:	:white_check_mark:	:white_check_mark:

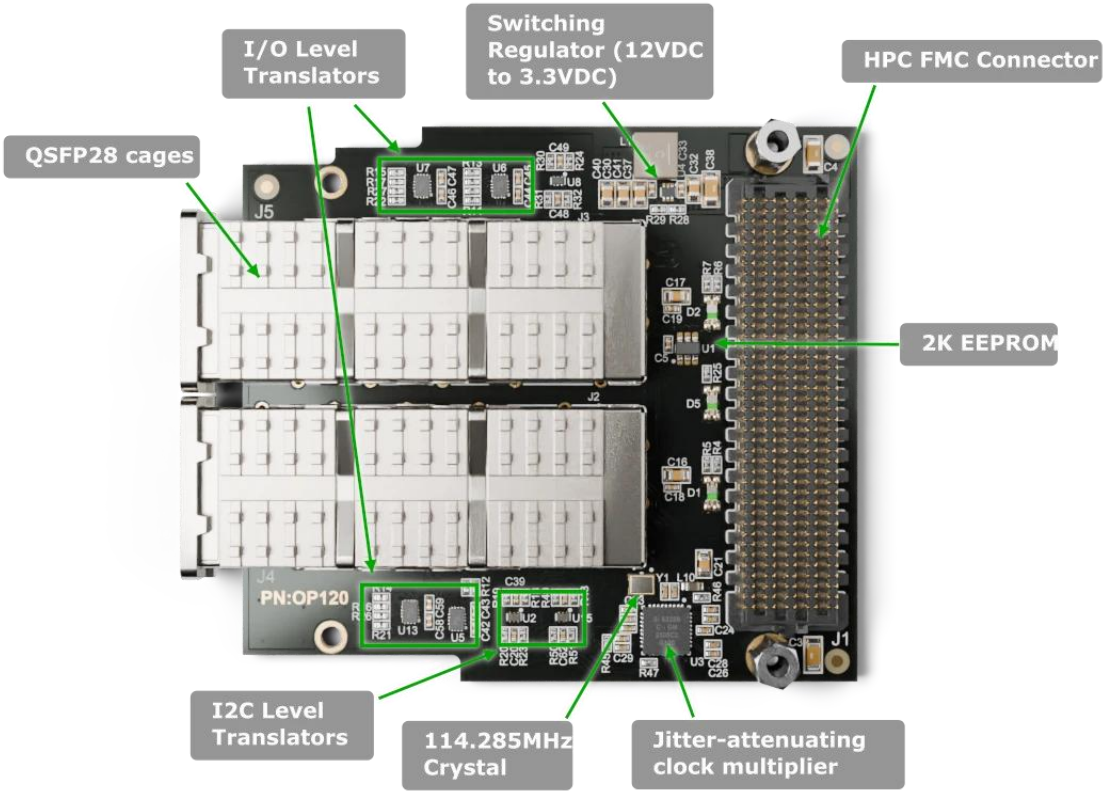
Certifications

- RoHS
- CE

Detailed Description

Hardware Overview

The figure below illustrates the various hardware components that are located on the top-side (component side) of the 2x QSFP28 FMC.

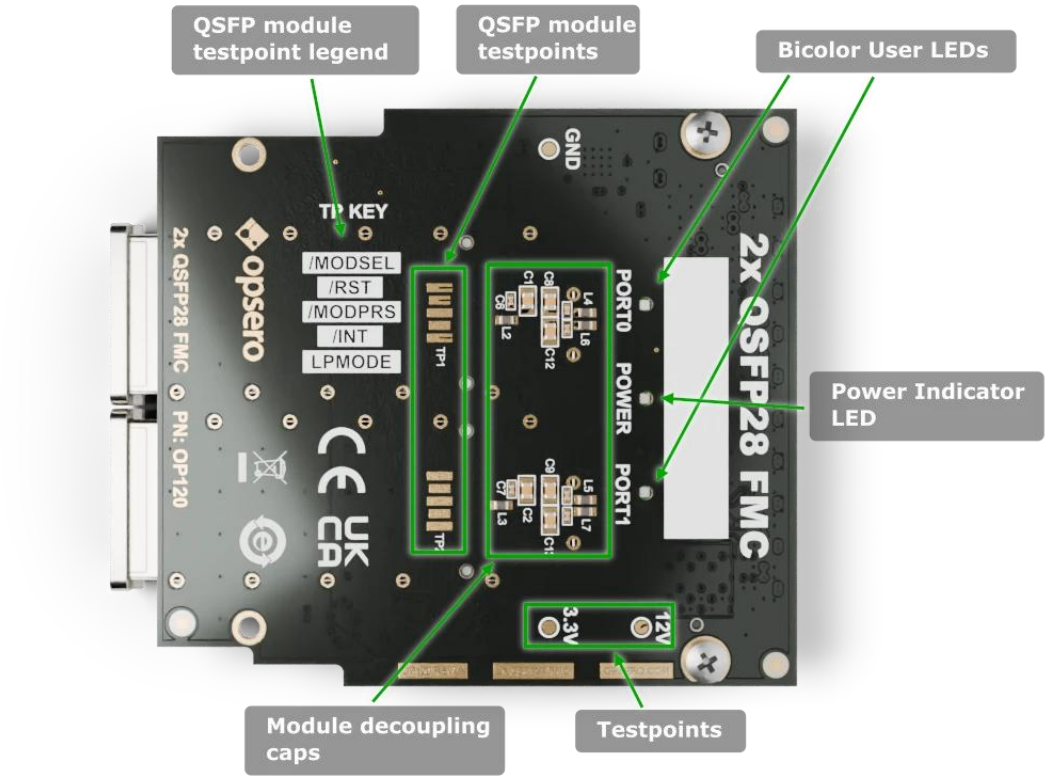


2x QSFP28 FMC labelled top-side

The main components on the top-side of the mezzanine card are:

- 2x QSFP28 cages
- High Pin Count FMC Connector
- 2K EEPROM
- Jitter-attenuating clock multiplier (Si5328)
- 114.285MHz crystal
- I2C Level translators
- I/O Level translators
- 3.3VDC switching buck regulator

The figure below illustrates the various hardware components that are located on the bottom-side of the mezzanine card.



2x QSFP28 FMC labelled bottom-side

The main components on the bottom-side of the mezzanine card are:

- Bicolor user LEDs
- FMC Power indicator LED
- Test points for 12VDC and 3.3VDC power supplies
- Test points for QSFP modules
- Legend for QSFP testpoints
- Decoupling capacitors for QSFP modules

QSFP28 Cages

The QSFP28 cages can accommodate 2x QSFP, QSFP+ or QSFP28 modules. Each QSFP28 module provides four lanes of up to 25 Gbps each, supporting an aggregate data rate of up to 100 Gbps per port.

<!-- TODO: Add QSFP28 cage datasheet reference when available -->

Jitter-attenuating Clock Multiplier

The 2x QSFP28 FMC features a jitter-attenuating clock multiplier (Skyworks, Si5328), which generates two precision clocks with selectable frequencies ranging from 8kHz to 808MHz. Its wide frequency range and exceptional jitter performance support a variety of applications, including Synchronous Ethernet.

The Si5328 utilizes a 114.285MHz crystal and oscillator circuit to generate frequencies between 8kHz and 808MHz. The clock multiplication ratio can be programmed through an I2C interface. The device also has a clock input, connected to FPGA I/O pins (LA00_CC_P/N), which can receive a recovered clock from the FPGA gigabit transceivers. In Synchronous Ethernet applications, jitter attenuation can be applied to the recovered clock, which can then be directed to the clock outputs to drive the gigabit transceivers.

See the Clocks section for more information on the clock system.

EEPROM

The 2K EEPROM stores IPMI FRU data that can be read by the carrier board and contains the following information:

- Manufacturer name (Opsero Electronic Design Inc.)
- Product name
- Product part number
- Serial number
- Power supply requirements

The FRU data is read by some carrier boards to determine the correct VADJ voltage to apply to the mezzanine card. All Opsero FMC products have their EEPROMs programmed with valid FRU data to allow these carrier boards to correctly power them.

Erasing or writing over the contents of the EEPROM can corrupt the IPMI FRU data making the mezzanine card unusable with carrier boards that require the information. We recommend that you do not use the mezzanine card's EEPROM for non-volatile storage but instead use the storage options provided by the carrier board. If you mistakenly erase or corrupt the contents of the EEPROM, you can reprogram it using the Opsero FMC EEPROM Tool. For more information, see: FMC EEPROM tool.

High Pin Count FMC Connector

The 2x QSFP28 FMC has a high pin count FMC (FPGA Mezzanine Card) connector for interfacing with an FPGA or SoC development board. The part number of this connector is Samtec, High pin count FMC connector, Module side, ASP-134488-01. The pinout of this connector conforms to the VITA 57.1 FPGA Mezzanine Card Standard. For the pinout details, see the Pin configuration section. For more information on the FMC connector and the VITA 57.1 standard, see the Samtec page on VITA 57.1.

I/O Interfaces

The FMC connector provides power to the 2x QSFP28 FMC and also presents the following I/O signals to the FPGA fabric of the development board:

- Gigabit serial links for the 2x QSFP28 slots (4 lanes per port, 8 lanes total)
- QSFP I/O signals (MODPRS_L, RESET_L, LPMODE, INT_L, MODSEL_L) for the 2x QSFP28 slots
- I2C for IPMI EEPROM
- I2C for each of the QSFP28 slots
- I2C for the clock multiplier
- LVDS recovered clock from the FPGA to drive the clock multiplier
- LVDS configurable clock from the clock multiplier
- Clock loss alarm from the clock multiplier
- Drive signals for the 2x bicolor user LEDs
- Reset signal for the I2C switch

The figure below illustrates the connections to the FMC connector.

<!-- TODO: Add FMC I/O interfaces block diagram (2x-qsfp28-fmc-fmc.png) when available -->

Details on the I2C connections can be found in the I2C Buses section.

The level translators have been left out of the above diagram for clarity. Details can be found in the Level translation section.

Level translation

To support a wide range of I/O voltages (VADJ), the 2x QSFP28 FMC uses level translators for the QSFP I/O signals, the I2C bus signals, the LED drive signals and the clock loss alarm signal. The table below lists the devices used:

Device	Purpose
TCA9416	Level translation of the PL I2C bus.
SN74AVC4T245RSVR	Level translation of QSFP I/Os, LED drive signals and clock loss alarm.

The gigabit serial links of the QSFP28 slots and the reference clocks connect to the gigabit transceivers, which are independent of the VADJ voltage and do not need voltage translation. The recovered clock signal (REC_CLK1_P/N) should be configured as an LVDS output in the FPGA and also does not require voltage translation.

Gigabit transceivers

The data channels between the QSFP28 modules and the FPGA operate over serial gigabit links at speeds of up to 25 Gbps per lane. Each QSFP28 module has four lanes, providing an aggregate bandwidth of up to 100 Gbps per port. The 2x QSFP28 FMC connects these serial links to gigabit transceivers in the FPGA or SoC on the development board. Each serial link consists of two differential pairs: one for transmission and one for reception. Port 0 connects to the first four gigabit transceivers on the FMC connector (DP0-3), and Port 1 connects to the next four gigabit transceivers (DP4-7).

QSFP28 Port	Lane	Signal direction	FMC gigabit transceiver
0	0	FPGA to link partner	DP0_C2M_P/N
		Link partner to FPGA	DP0_M2C_P/N
	1	FPGA to link partner	DP1_C2M_P/N
		Link partner to FPGA	DP1_M2C_P/N
	2	FPGA to link partner	DP2_C2M_P/N
		Link partner to FPGA	DP2_M2C_P/N

	3	FPGA to link partner	DP3_C2M_P/N
		Link partner to FPGA	DP3_M2C_P/N
1	0	FPGA to link partner	DP4_C2M_P/N
		Link partner to FPGA	DP4_M2C_P/N
	1	FPGA to link partner	DP5_C2M_P/N
		Link partner to FPGA	DP5_M2C_P/N
	2	FPGA to link partner	DP6_C2M_P/N
		Link partner to FPGA	DP6_M2C_P/N
	3	FPGA to link partner	DP7_C2M_P/N
		Link partner to FPGA	DP7_M2C_P/N

As the serial links connect to gigabit transceivers, they are independent of the VADJ voltage being used and do not need voltage translation.

QSFP I/O Signals

In addition to the high-speed serial links, QSFP28 modules have several management I/O signals used for configuration, status indication and fault management. On the 2x QSFP28 FMC, these I/O signals are connected through level translators to the FPGA I/O, allowing the FPGA to control and read them. The I/O signals and their functionality are listed in the table below:

QSFP pin	Name	Direction	Function
27	MODPRS_L	QSFP to FPGA	Indicates module presence (active low)
28	INT_L	QSFP to FPGA	Indicates module interrupt (active low)
8	MODSEL_L	FPGA to QSFP	Selects the module for I2C communication (active low)

9	RESET_L	FPGA to QSFP	Resets the module (active low)
31	LPMODE	FPGA to QSFP	Sets the module to low power mode

The QSFP I/O signals connect to the FMC pins listed in the table below:

Port	Net Name	FMC pin
0	QSFP0_MODPRS_L_T	LA12_P
	QSFP0_INT_L_T	LA12_N
	QSFP0_MODSEL_L_T	LA04_P
	QSFP0_RESET_L_T	LA04_N
	QSFP0_LPMODE_T	LA11_P
1	QSFP1_MODPRS_L_T	LA05_P
	QSFP1_INT_L_T	LA05_N
	QSFP1_MODSEL_L_T	LA15_P
	QSFP1_RESET_L_T	LA15_N
	QSFP1_LPMODE_T	LA11_N

I2C Buses

The 2x QSFP28 FMC has four independent I2C buses: the FMC's dedicated I2C bus for the IPMI EEPROM and three PL (programmable logic) I2C buses that connect to the 2x QSFP modules and the clock multiplier.

EEPROM I2C

A 2K EEPROM is located on the FMC card's dedicated I2C bus. The FMC pins of the I2C bus are shown below, and it is up to the user to determine their corresponding connections to the FPGA/MPSoC on the carrier board being used.

I2C bus signal	FMC pin name	FMC pin number

SCL (clock)	SCL	C30
SDA (data)	SDA	C31

Be aware that on some carrier boards, the FMC I2C bus passes through an I2C MUX. On some boards it connects to FPGA pins whereas on others it connects to PS pins. If you wish to communicate with the EEPROM or I/O expander, it is necessary to check the schematic drawing of your carrier board to determine the structure of the I2C bus and to which pins it connects.

CLK I2C

The clock multiplier I2C bus of the 2x QSFP28 FMC is implemented using two FPGA I/O pins (LA02_P/N) and enables communication between the FPGA and the clock multiplier. The I2C bus signals are connected to the FMC pins listed in the table below:

Net Name	Description	FMC pin
CLK_I2C_SCL_T	I2C clock (SCL)	LA02_P
CLK_I2C_SDA_T	I2C data (SDA)	LA02_N

The CLK I2C bus signals pass through a level translator to convert the FPGA I/O levels (VADJ) to 3.3VDC levels.

QSFP0/1 I2C

The 2x QSFP28 FMC has two independent I2C busses to enable communication between the FPGA and the QSFP modules. The I2C bus signals are connected to the FMC pins listed in the table below:

Port	Net Name	Description	FMC pin
QSFP0	QSFP0_I2C_SCL_T	I2C clock (SCL)	LA03_P
	QSFP0_I2C_SDA_T	I2C data (SDA)	LA03_N
QSFP1	QSFP1_I2C_SCL_T	I2C clock (SCL)	LA17_CC_P
	QSFP1_I2C_SDA_T	I2C data (SDA)	LA17_CC_N

The QSFP0/1 I2C bus signals pass through a level translator to convert the FPGA I/O levels (VADJ) to 3.3VDC levels.

Clock signals

Refer to the Clocks section for more information about the clock related signals and how they connect to the jitter-attenuating clock multiplier.

Bicolor User LEDs

The 2x QSFP28 FMC features two bicolor (green/red) LEDs, one for each QSFP28 port, which can be driven by the FPGA and are visible on the bottom side of the mezzanine card. These LEDs provide the user or developer with programmable visible outputs that can be linked to specific signals for monitoring. Examples of such signals for monitoring include the QSFP I/Os (MODPRS_L, INT_L, RESET_L, LPMODE) or other QSFP module-specific indicators.

The drive pins for the user LEDs are routed through level translators to convert the FPGA I/O signal levels (VADJ) to 3.3VDC levels for driving the LEDs. The level translators have sufficient output current capacity to drive the LEDs directly.

The bicolor user LEDs connect to the FMC pins listed in the table below:

Aligned with port	Net Name	FMC pin
0	QSFP0_GRN_LED_T	LA07_P
	QSFP0_RED_LED_T	LA07_N
1	QSFP1_GRN_LED_T	LA08_P
	QSFP1_RED_LED_T	LA08_N

Note that when the green and red signals for a single LED are asserted at the same time, the resulting color is amber.

Power Supplies

All power required by the 2x QSFP28 FMC is supplied by the development board through the FMC connector:

- +12VDC
- VADJ: +1.2VDC, +1.5VDC, +1.8VDC, +2.5VDC or +3.3VDC
- +3.3VAUX

<!-- TODO: Add power supplies block diagram (2x-qsfp28-fmc-power.png) when available -->

The FPGA/MPSoC carrier board also supplies a 3.3VDC power supply, however this supply is not used by the 2x QSFP28 FMC.

The 12VDC Supply

The 12VDC supply is the main power source for the mezzanine card. It feeds a buck switching regulator (TI, 3-16V 5A Buck Converter, TPS565247DRLR) that generates 3.3VDC to power to both QSFP28 slots, the clock multiplier and the level translators.

VADJ Supply

The VADJ supply is the FPGA I/O power supply and it determines the voltage levels of the FMC I/Os. On the 2x QSFP28 FMC, the VADJ supply powers the level translators that allow the board to be used at any I/O voltage in the range of 1.2VDC to 3.3VDC.

The 3.3VAUX Supply

The 3.3VAUX supply is used to power the IPMI EEPROM and is independent of the main 3.3VDC supply so that the carrier board can read from the EEPROM without having to power up the entire board.

Power LED and testpoints

An LED indicates when both the power from the carrier board and the switching regulator are active, and it can be seen in the labelled bottom view of the board above. This LED is connected through a logic buffer to the POWER GOOD signal that is driven by the carrier board and is part of the Vita 57.1 FMC standard. The logic buffer is powered by the 3.3VDC that is generated by the switching regulator.

To aid hardware debug, there is a test point for the 12VDC and 3.3VDC (buck regulator) power supplies on the back side of the 2x QSFP28 FMC.

Clocks

The clock architecture of the 2x QSFP28 FMC is based on the jitter-attenuating clock multiplier (Skyworks, Si5328). This clock multiplier operates in a free-running mode, generating a user-specified frequency ranging from 8kHz to 808MHz, synthesized by a crystal oscillator. In Synchronous Ethernet applications, it can also generate a jitter attenuated clock that is synchronous with link partner's clock.

The figure below illustrates the clock connections on the 2x QSFP28 FMC.

<!-- TODO: Add clocks block diagram (2x-qsfp28-fmc-clocks.png) when available -->

Clock outputs

The Si5328 has two output clocks, both connected to the FMC connector's GT reference clock inputs. These clocks are divided down separately from a common source, allowing them to be programmed to different frequencies while remaining synchronous.

The clock outputs are connected to the FMC pins listed in the table below:

Si5328 pin	I/O standard	FMC pin
CLKOUT1	LVDS	GBTCLK0_M2C_P/N
CLKOUT2	LVDS	GBTCLK1_M2C_P/N

Clock input

The Si5328 has two input clocks, but only one is connected on the 2x QSFP28 FMC. This clock input is connected to the FMC pins LA00_CC_P/N, enabling the FPGA to forward a recovered clock from the gigabit transceivers. The Si5328 can perform jitter attenuation on the recovered clock and forward the resulting clock to its outputs. This feature allows the 2x QSFP28 FMC to be used in Synchronous Ethernet applications.

The clock inputs are connected to the FMC pins listed in the table below:

Si5328 pin	I/O standard	FMC pin
CLKIN1	LVDS	LA00_CC_P/N

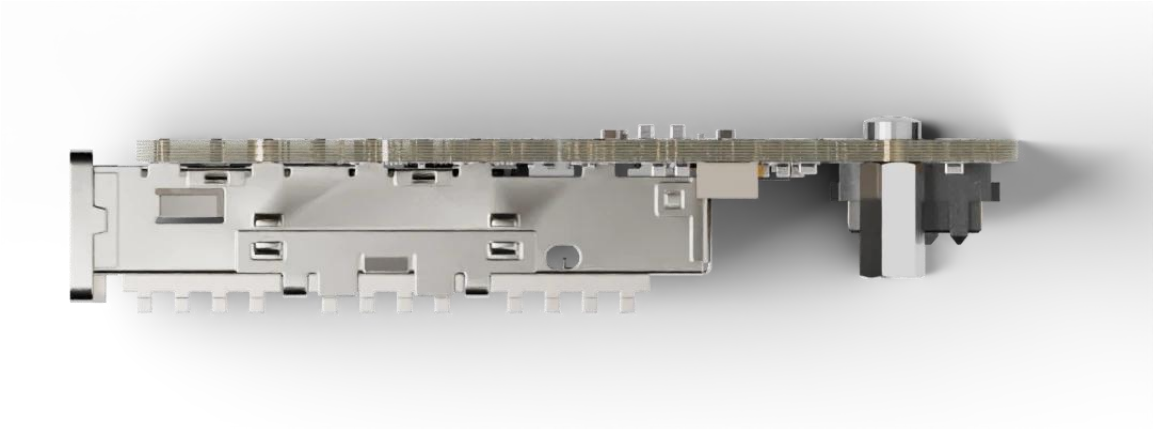
Clock loss alarm

The Si5328 has a logic output INT_C1B that indicates loss-of-signal on the input clock CLKIN1 (the recovered clock). The signal goes HIGH when the device detects missing pulses on the input clock. The clock loss alarm passes through level translation and connects to FMC pin LA06_P.

Mechanical Information

Height Profile

The figure below illustrates the height profile of the 2x QSFP28 FMC.

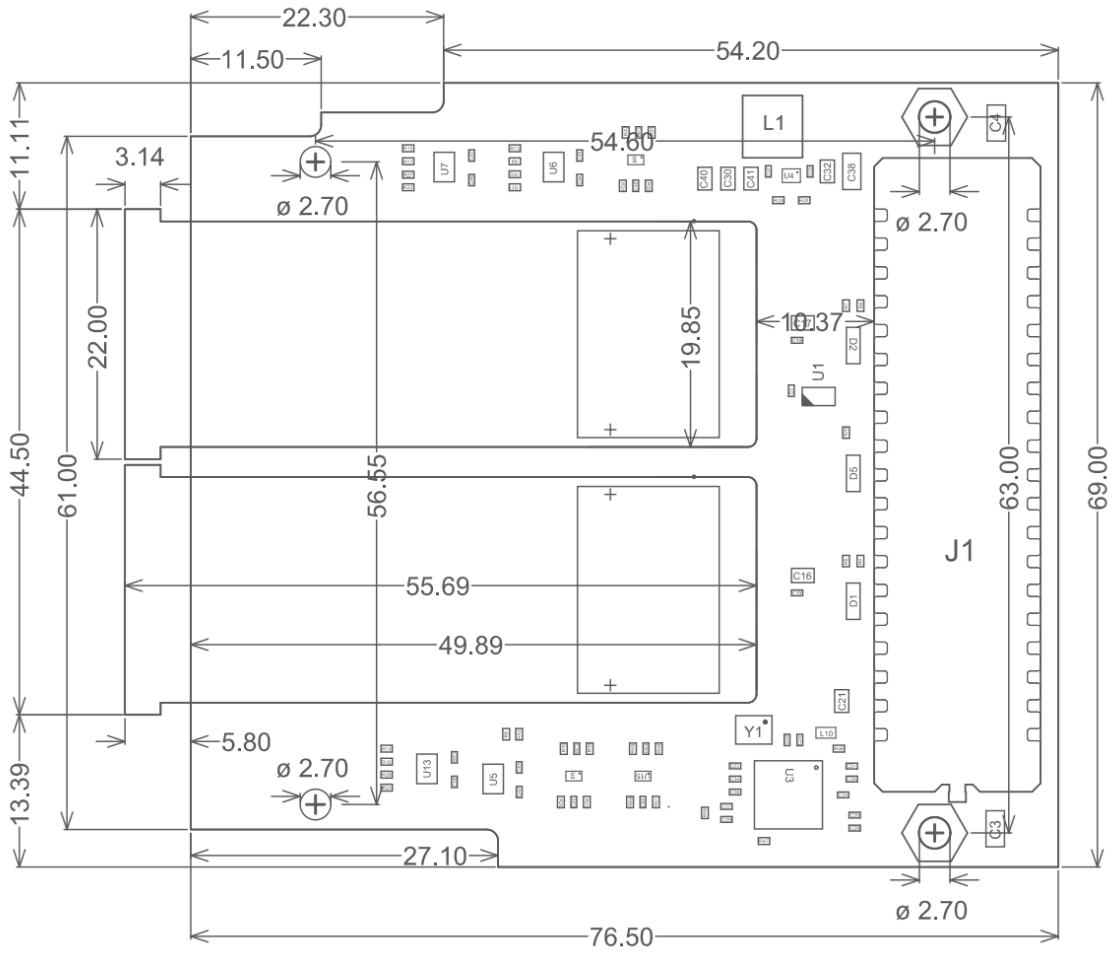


2x QSFP28 FMC profile

The QSFP28 cages are supplied with removable heat sinks attached. With the heat sinks in place, the total height of the cages exceeds the standard 10mm gap between the FMC card and the development board. This does not cause an issue with most AMD development boards, as their FMC connectors are positioned so that the mezzanine card overhangs the edge of the board, leaving plenty of room for the heat sinks. However, if using this mezzanine card with development boards that extend far enough to touch the heat sink, the heat sink must be removed to avoid mechanical interference and to ensure proper mating of the FMC connectors. If the heat sinks are removed, the user must ensure that adequate thermal management is provided by other means.

Dimensions

The mechanical dimensions of the 2x QSFP28 FMC are illustrated in the figure below. All dimensions are in millimeters (mm).



2x QSFP28 FMC dimensions

The assembly drawings are also available as PDF files that you can download at the provided links.

- 2x QSFP28 FMC Rev-A Assembly Drawing PDF

The 3D Model

The 3D model of the board is available as a STEP file at the links below:

- 2x QSFP28 FMC Rev-A 3D STEP model

Mezzanine fastening hardware

For mechanical fastening of the mezzanine card to the carrier board, the 2x QSFP28 FMC comes with 2x hex standoffs. We **highly recommend** using the machine screws on each of these standoffs to fix the mezzanine card to the carrier board. If the fastening screws are misplaced, they can be replaced by the ones listed below, or equivalents.

The hex standoff and machine screw part numbers are listed below:

- Hex standoff, Thread M2.5 x 0.45, Brass, Board-to-board length 10mm **Part number:** V6516C **Manufacturer:** Assmann
- Machine screw, Thread M2.5 x 0.45, Length (below head) 4mm, Stainless steel, Phillips head **Part number:** 90116A105 **Supplier:** McMaster-Carr

Compatible Boards

This section of the documentation aims to list all of the development boards for which compatibility with the 2x QSFP28 FMC has been checked, and to list constraints and any notes concerning special requirements or limitations with the board.

The 2x QSFP28 FMC requires 8 gigabit transceivers (DP0-DP7) to support both QSFP28 ports. Low pin count (LPC) FMC connectors only provide a single transceiver (DP0) and therefore **cannot support** any QSFP28 port on this mezzanine card. A high pin count (HPC) or FMC+ connector with at least DP0-DP3 routed is required to use Port 0 (1 port), and DP0-DP7 routed is required to use both ports.

List of boards

The following development boards have been verified compatible with the 2x QSFP28 FMC. For more detailed information regarding compatibility with a particular development board, including the availability of an example design, click on the name of the board in the table below.

Zynq Ultrascale+ boards

Carrier	FMC	Compatible	Ref design	Supported Ports	Supported Link Speed
AMD Xilinx ZCU102 Zynq	HPC0	:white_check_mark:	Coming soon	2	2x 40G

UltraScale+ Development board					
AMD Xilinx ZCU102 Zynq UltraScale+ Development board	HPC1	:white_check_mark:	Coming soon	2	2x 40G
AMD Xilinx ZCU106 Zynq UltraScale+ Development board	HPC0	:white_check_mark:	Coming soon	2	2x 40G
AMD Xilinx ZCU111 Zynq UltraScale+ Development board	FMC+	:white_check_mark:	Coming soon	2	2x 100G
AMD Xilinx ZCU208 Zynq UltraScale+ Development board	FMC+	:white_check_mark:	Coming soon	2	2x 100G
AMD Xilinx ZCU216 Zynq	FMC+	:white_check_mark:	Coming soon	2	2x 100G

UltraScale+ Development board					
Avnet UltraZed EV Carrier Zynq UltraScale+ Development board	HPC	:white_check_mark:	Coming soon	2	2x 40G

Ultrascale+ boards

Carrier	FMC	Compatible	Ref design	Supported Ports	Supported Link Speed
AMD Xilinx VCU118 Virtex UltraScale+ Development board	FMC+	:white_check_mark:	Coming soon	2	2x 40G

Versal boards

Carrier	FMC	Compatible	Ref design	Supported Ports	Supported Link Speed
AMD Xilinx VCK190 Versal AI Core Development board	FMC+1	:white_check_mark:	Coming soon	2	2x 100G

AMD Xilinx VCK190 Versal AI Core Development board	FMC+2	:white_check_mark:	Coming soon	2	2x 100G
AMD Xilinx VEK280 Versal AI Edge Development board	FMC+	:white_check_mark:	Coming soon	2	2x 100G
AMD Xilinx VHK158 Versal HBM Series Development board	FMC+	:white_check_mark:	Coming soon	2	2x 100G
AMD Xilinx VMK180 Versal Prime Series Development board	FMC+1	:white_check_mark:	Coming soon	2	2x 100G
AMD Xilinx VMK180 Versal Prime Series Development board	FMC+2	:white_check_mark:	Coming soon	2	2x 100G

AMD Xilinx VPK120 Versal Premium Series Development board	FMC+	:white_check_mark:	Coming soon	2	2x 100G
AMD Xilinx VPK180 Versal Premium Series Development board	FMC+	:white_check_mark:	Coming soon	2	2x 100G

Compatibility requirements

If you need to determine the compatibility of a development board that is not listed here, or you are designing a carrier board to mate with the 2x QSFP28 FMC, please check your board against the list of requirements below.

VADJ

The development board must have the ability to supply a VADJ voltage between 1.2VDC and 3.3VDC. The 2x QSFP28 FMC has an EEPROM containing IPMI data to be used by a power management device. If the development board has such a power management device, an appropriate VADJ voltage will be applied automatically on power-up. Note that some development boards require the VADJ voltage to be configured by a DIP switch or jumper placement.

Gigabit transceivers

The FPGA or MPSoC device must have gigabit transceivers and they must be routed to the FMC connector. Each QSFP28 port requires four gigabit transceivers. Port 0 uses DP0-DP3 and Port 1 uses DP4-DP7. All eight transceivers must be connected to the FPGA for both QSFP28 ports to work.

Port	Lane	Signal direction	FMC Pin	FMC pin name
0	0	Link partner to FPGA	C6/C7	DP0_M2C_P/N
		FPGA to Link partner	C2/C3	DP0_C2M_P/N
0	1	Link partner to FPGA	A2/A3	DP1_M2C_P/N
		FPGA to Link partner	A22/A23	DP1_C2M_P/N
0	2	Link partner to FPGA	A6/A7	DP2_M2C_P/N
		FPGA to Link partner	A26/A27	DP2_C2M_P/N
0	3	Link partner to FPGA	A10/A11	DP3_M2C_P/N
		FPGA to Link partner	A30/A31	DP3_C2M_P/N
1	0	Link partner to FPGA	A14/A15	DP4_M2C_P/N
		FPGA to Link partner	A34/A35	DP4_C2M_P/N
1	1	Link partner to FPGA	A18/A19	DP5_M2C_P/N
		FPGA to Link partner	A38/A39	DP5_C2M_P/N

1	2	Link partner to FPGA	B16/B17	DP6_M2C_P/N
		FPGA to Link partner	B36/B37	DP6_C2M_P/N
1	3	Link partner to FPGA	B12/B13	DP7_M2C_P/N
		FPGA to Link partner	B32/B33	DP7_C2M_P/N

Note that low pin count (LPC) FMC connectors only have one possible GT connection (DP0). Since each QSFP28 port requires four GT lanes, LPC FMC connectors are **not compatible** with the 2x QSFP28 FMC.

At least one of the GT clock references (FMC pins GBTCLK0_M2C_P/N and GBTCLK1_M2C_P/N) should be connected to one of the GT reference clock inputs of the quad to which DP0-7 connect, or an adjacent quad.

Required I/O

The following FMC pins **must** be connected to the FPGA as they provide critical I/O to the mezzanine card.

FMC Pin	FMC name	Net	Description
H7	LA02_P	CLK_I2C_SCL_T	Clock multiplier I2C bus clock SCL
H8	LA02_N	CLK_I2C_SDA_T	Clock multiplier I2C bus data SDA
G9	LA03_P	QSFP0_I2C_SCL_T	Port 0: I2C Clock
G10	LA03_N	QSFP0_I2C_SDA_T	Port 0: I2C Data (bidirectional)
D20	LA17_P_CC	QSFP1_I2C_SCL_T	Port 1: I2C Clock

D21	LA17_N_CC	QSFP1_I2C_SDA_T	Port 1: I2C Data (bidirectional)
H10	LA04_P	QSFP0_MODSELL_T	Port 0: Module Select (active low)
H11	LA04_N	QSFP0_RESETL_T	Port 0: Reset (active low)
H19	LA15_P	QSFP1_MODSELL_T	Port 1: Module Select (active low)
H20	LA15_N	QSFP1_RESETL_T	Port 1: Reset (active low)

Featured I/O

The following FMC pins should ideally be connected to the FPGA as they provide extra functionality to the mezzanine card. These pins are not critical to the operation of the mezzanine card; it can operate without them if they are not connected on the carrier board.

FMC Pin	FMC name	Net	Description
G15	LA12_P	QSFP0_MODPRSL_T	Port 0: Module Present (active low)
G16	LA12_N	QSFP0_INTL_T	Port 0: Interrupt (active low)
D11	LA05_P	QSFP1_MODPRSL_T	Port 1: Module Present (active low)
D12	LA05_N	QSFP1_INTL_T	Port 1: Interrupt (active low)
H16	LA11_P	QSFP0_LPMODE_T	Port 0: Low Power Mode
H17	LA11_N	QSFP1_LPMODE_T	Port 1: Low Power Mode

G12	LA08_P	QSFP1_GRN_LED_T	Port 1: User bicolor LED Green
G13	LA08_N	QSFP1_RED_LED_T	Port 1: User bicolor LED Red
H13	LA07_P	QSFP0_GRN_LED_T	Port 0: User bicolor LED Green
H14	LA07_N	QSFP0_RED_LED_T	Port 0: User bicolor LED Red
G6	LA00_P_CC	REC_CLK1_P	Recovered clock positive (LVDS, FPGA to Si5328)
G7	LA00_N_CC	REC_CLK1_N	Recovered clock negative (LVDS, FPGA to Si5328)
C10	LA06_P	CLK_LOS_ALARM_T	Clock loss alarm from Si5328

Board Revision History

Rev A

- First boards manufactured

Rev B

- First commercial release
- Rev B was designed to improve the signal integrity of the first revision and improve yield
- Copper layers increased to 12 (from 8)
- I2C voltage translators changed to TCA9416DDFR to improve manufacturing yield

Ordering Information

Vendor	Part name	Part number
Opsero	2x QSFP28 FMC	OP120
Digi-Key	2x QSFP28 FMC	OP120

Revision History

Date	Version	Description
2026-04-21	1.0	Initial PDF release.

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