MCIO PCIe FMC Datasheet

Part number: OP103

Overview

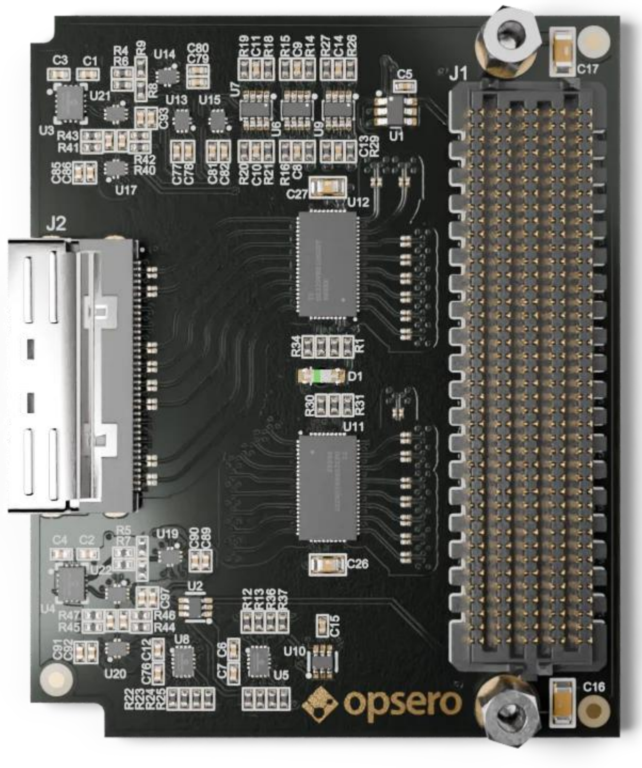
Description

The MCIO PCIe FMC is an FPGA Mezzanine Card designed to bring high-speed MCIO PCIe connectivity to FPGA and MPSoC development boards. It connects to the development board via a high pin count (HPC) FMC connector and provides an 8-lane MCIO PCIe connector with all 8 lanes routed to gigabit transceivers on the FMC interface. The card supports PCIe Gen4 speeds (16 GT/s per lane) and incorporates two TI PCIe redrivers (TI, 8-lane PCIe Gen4 Redriver, DS320PR810) to compensate for signal loss across MCIO cables and adapters.

Unlike the MCIO PCIe Host FMC (OP100), which is limited to host mode, the MCIO PCIe FMC can operate in both **host mode** and **device mode**. The operating mode is selected by a logic signal on the FMC connector, allowing the carrier board's FPGA to select the mode on configuration.

The 8-lane interface can also be used as a dual 4-lane (2x4) configuration, providing flexibility for applications that require two independent PCIe links.

Top view



MCIO PCIe FMC top

Bottom view

MCIO PCIe FMC bottom

Features

- 8-lane MCIO PCIe connector with all 8 lanes routed
- Supports both host and device modes, switchable via FPGA logic signal
- Supports up to PCIe Gen4 speeds (16 GT/s per lane)
- Dual 4-lane (2x4) configuration capability
- Two TI TI, 8-lane PCIe Gen4 Redriver, [DS320PR810] PCIe redrivers for signal integrity
- High Pin Count (HPC) FMC connector conforming to [VITA 57.1 FMC Standard]
- Adjustable I/O voltage (VADJ) range: 1.2V to 3.3V
- Level translators for broad voltage compatibility

- 2K EEPROM with IPMI FRU data for automatic VADJ configuration

Typical applications

- Connecting FPGA development boards to PCIe devices via MCIO cables
- Exposing an FPGA as a PCIe endpoint device to a host system
- PCIe link testing and protocol analysis
- High-speed data transfer between FPGA and external PCIe systems or other FPGAs

Supported development boards

For a list of all the FPGA and MPSoC development boards that are compatible with the MCIO PCIe FMC, please refer to the list of compatible boards.

The carrier board must have gigabit transceivers routed to the FMC connector (DP0-DP7 pins) and must be capable of supplying a VADJ voltage in the range 1.2V to 3.3V.

Ordering

The MCIO PCIe FMC can be ordered from the vendors listed below. The links under the part number column will take you to the corresponding order page.

Vendor	Part name	Part number
Opsero	MCIO PCIe FMC	OP103

Included with the MCIO PCIe FMC are:

- 2x machine screws for fixing the mezzanine card to the carrier card

Pin Configuration

Pinout table

The MCIO PCIe FMC has a high pin count FPGA Mezzanine Card (FMC) connector, providing the connections to the FPGA on the development board. The following table defines the pinout of the FMC connector and describes each pin's purpose on this mezzanine card.

The PCIe nets have been labelled as follows:

- PERA: PCIe RX for MCIO Channel A
- PETA: PCIe TX for MCIO Channel A
- PERB: PCIe RX for MCIO Channel B
- PETB: PCIe TX for MCIO Channel B

Note that although the 8xMCIO connector is divided into two channels A and B, it can also be used as a single 8-lane PCIe connection.

Pin	Pin name	Net	Description
A1	GND	GND	Ground
A2	DP1_M2C_P	PERA_1_P	PCIe lane 1 positive (MCIOA-to-FPGA)
A3	DP1_M2C_N	PERA_1_N	PCIe lane 1 negative (MCIOA-to-FPGA)
A4	GND	GND	Ground
A5	GND	GND	Ground
A6	DP2_M2C_P	PERA_2_P	PCIe lane 2 positive (MCIOA-to-FPGA)
A7	DP2_M2C_N	PERA_2_N	PCIe lane 2 negative (MCIOA-to-FPGA)
A8	GND	GND	Ground
A9	GND	GND	Ground
A10	DP3_M2C_P	PERA_3_P	PCIe lane 3 positive (MCIOA-to-FPGA)
A11	DP3_M2C_N	PERA_3_N	PCIe lane 3 negative (MCIOA-to-FPGA)

A12	GND	GND	Ground
A13	GND	GND	Ground
A14	DP4_M2C_P	PERB_0_P	PCIe lane 0 positive (MCIOB-to-FPGA)
A15	DP4_M2C_N	PERB_0_N	PCIe lane 0 negative (MCIOB-to-FPGA)
A16	GND	GND	Ground
A17	GND	GND	Ground
A18	DP5_M2C_P	PERB_1_P	PCIe lane 1 positive (MCIOB-to-FPGA)
A19	DP5_M2C_N	PERB_1_N	PCIe lane 1 negative (MCIOB-to-FPGA)
A20	GND	GND	Ground
A21	GND	GND	Ground
A22	DP1_C2M_P	PETA_1_P	PCIe lane 1 positive (FPGA-to-MCIOA)
A23	DP1_C2M_N	PETA_1_N	PCIe lane 1 negative (FPGA-to-MCIOA)
A24	GND	GND	Ground
A25	GND	GND	Ground
A26	DP2_C2M_P	PETA_2_P	PCIe lane 2 positive (FPGA-to-MCIOA)
A27	DP2_C2M_N	PETA_2_N	PCIe lane 2 negative (FPGA-to-MCIOA)
A28	GND	GND	Ground

A29	GND	GND	Ground
A30	DP3_C2M_P	PETA_3_P	PCIe lane 3 positive (FPGA-to-MCIOA)
A31	DP3_C2M_N	PETA_3_N	PCIe lane 3 negative (FPGA-to-MCIOA)
A32	GND	GND	Ground
A33	GND	GND	Ground
A34	DP4_C2M_P	PETB_0_P	PCIe lane 0 positive (FPGA-to-MCIOB)
A35	DP4_C2M_N	PETB_0_N	PCIe lane 0 negative (FPGA-to-MCIOB)
A36	GND	GND	Ground
A37	GND	GND	Ground
A38	DP5_C2M_P	PETB_1_P	PCIe lane 1 positive (FPGA-to-MCIOB)
A39	DP5_C2M_N	PETB_1_N	PCIe lane 1 negative (FPGA-to-MCIOB)
A40	GND	GND	Ground
B1	CLK_DIR	N/C	Not connected
B2	GND	GND	Ground
B3	GND	GND	Ground
B4	DP9_M2C_P	N/C	Not connected
B5	DP9_M2C_N	N/C	Not connected
B6	GND	GND	Ground
B7	GND	GND	Ground

B8	DP8_M2C_P	N/C	Not connected
B9	DP8_M2C_N	N/C	Not connected
B10	GND	GND	Ground
B11	GND	GND	Ground
B12	DP7_M2C_P	PERB_3_P	PCIe lane 3 positive (MCIOB-to-FPGA)
B13	DP7_M2C_N	PERB_3_N	PCIe lane 3 negative (MCIOB-to-FPGA)
B14	GND	GND	Ground
B15	GND	GND	Ground
B16	DP6_M2C_P	PERB_2_P	PCIe lane 2 positive (MCIOB-to-FPGA)
B17	DP6_M2C_N	PERB_2_N	PCIe lane 2 negative (MCIOB-to-FPGA)
B18	GND	GND	Ground
B19	GND	GND	Ground
B20	GBTCLK1_M2C_P	CLKB_F_P	100MHz PCIe reference clock for the FPGA
B21	GBTCLK1_M2C_N	CLKB_F_N	100MHz PCIe reference clock for the FPGA
B22	GND	GND	Ground
B23	GND	GND	Ground
B24	DP9_C2M_P	N/C	Not connected

B25	DP9_C2M_N	N/C	Not connected
B26	GND	GND	Ground
B27	GND	GND	Ground
B28	DP8_C2M_P	N/C	Not connected
B29	DP8_C2M_N	N/C	Not connected
B30	GND	GND	Ground
B31	GND	GND	Ground
B32	DP7_C2M_P	PETB_3_P	PCIe lane 3 positive (FPGA-to-MCIOB)
B33	DP7_C2M_N	PETB_3_N	PCIe lane 3 negative (FPGA-to-MCIOB)
B34	GND	GND	Ground
B35	GND	GND	Ground
B36	DP6_C2M_P	PETB_2_P	PCIe lane 2 positive (FPGA-to-MCIOB)
B37	DP6_C2M_N	PETB_2_N	PCIe lane 2 negative (FPGA-to-MCIOB)
B38	GND	GND	Ground
B39	GND	GND	Ground
B40	RES0	N/C	Not connected
C1	GND	GND	Ground
C2	DP0_C2M_P	PETA_0_P	PCIe lane 0 positive (FPGA-to-MCIOA)
C3	DP0_C2M_N	PETA_0_N	PCIe lane 0 negative (FPGA-to-MCIOA)

C4	GND	GND	Ground
C5	GND	GND	Ground
C6	DP0_M2C_P	PERA_0_P	PCIe lane 0 positive (MCIOA-to-FPGA)
C7	DP0_M2C_N	PERA_0_N	PCIe lane 0 negative (MCIOA-to-FPGA)
C8	GND	GND	Ground
C9	GND	GND	Ground
C10	LA06_P	N/C	Not connected
C11	LA06_N	N/C	Not connected
C12	GND	GND	Ground
C13	GND	GND	Ground
C14	LA10_P	SBA_DISABLE_T	Disable sideband A signals
C15	LA10_N	SBB_DISABLE_T	Disable sideband B signals
C16	GND	GND	Ground
C17	GND	GND	Ground
C18	LA14_P	HOST_MODE_N_T	Host mode enable active-low (0:HOST MODE, 1:DEVICE MODE)
C19	LA14_N	LOCAL_CLKS_N_T	Local/remote clock select (0:LOCAL, 1:REMOTE)

C20	GND	GND	Ground
C21	GND	GND	Ground
C22	LA18_P_CC	N/C	Not connected
C23	LA18_N_CC	N/C	Not connected
C24	GND	GND	Ground
C25	GND	GND	Ground
C26	LA27_P	N/C	Not connected
C27	LA27_N	N/C	Not connected
C28	GND	GND	Ground
C29	GND	GND	Ground
C30	SCL	I2C_SCL	I2C Clock (FPGA-to-PHY)
C31	SDA	I2C_SDA	I2C Data (bidirectional)
C32	GND	GND	Ground
C33	GND	GND	Ground
C34	GA0	GA0	EEPROM Address Bit 1 (A1)
C35	12P0V_1	12V0	12VDC
C36	GND	GND	Ground
C37	12P0V_2	12V0	12VDC
C38	GND	GND	Ground
C39	3P3V_1	3V3	3.3VDC
C40	GND	GND	Ground

D1	PG_C2M	PG	Power Good (Driven by carrier)
D2	GND	GND	Ground
D3	GND	GND	Ground
D4	GBTCLK0_M2C_P	CLKA_F_P	100MHz PCIe reference clock for the FPGA
D5	GBTCLK0_M2C_N	CLKA_F_N	100MHz PCIe reference clock for the FPGA
D6	GND	GND	Ground
D7	GND	GND	Ground
D8	LA01_P_CC	N/C	Not connected
D9	LA01_N_CC	N/C	Not connected
D10	GND	GND	Ground
D11	LA05_P	N/C	Not connected
D12	LA05_N	N/C	Not connected
D13	GND	GND	Ground
D14	LA09_P	N/C	Not connected
D15	LA09_N	N/C	Not connected
D16	GND	GND	Ground
D17	LA13_P	N/C	Not connected
D18	LA13_N	N/C	Not connected
D19	GND	GND	Ground

D20	LA17_P_CC	N/C	Not connected
D21	LA17_N_CC	N/C	Not connected
D22	GND	GND	Ground
D23	LA23_P	N/C	Not connected
D24	LA23_N	N/C	Not connected
D25	GND	GND	Ground
D26	LA26_P	N/C	Not connected
D27	LA26_N	N/C	Not connected
D28	GND	GND	Ground
D29	TCK	N/C	Not used
D30	TDI	TDI-TDO	JTAG TDI (Connects to TDO to close JTAG chain)
D31	TDO	TDI-TDO	JTAG TDO (Connects to TDI to close JTAG chain)
D32	3P3VAUX	3V3AUX	3.3VDC Power supply for EEPROM
D33	TMS	N/C	Not used
D34	TRST_L	N/C	Not used
D35	GA1	GA1	EEPROM Address Bit 0 (A0)
D36	3P3V_2	3V3	3.3VDC
D37	GND	GND	Ground
D38	3P3V_3	3V3	3.3VDC

D39	GND	GND	Ground
D40	3P3V_4	3V3	3.3VDC
G1	GND	GND	Ground
G2	CLK1_M2C_P	N/C	Not used
G3	CLK1_M2C_N	N/C	Not used
G4	GND	GND	Ground
G5	GND	GND	Ground
G6	LA00_P_CC	PERSTA_N_T	PCIe reset for MCIOA (active LOW)
G7	LA00_N_CC	CPRSNTA_N_T	PCIe detect for MCIOA
G8	GND	GND	Ground
G9	LA03_P	N/C	Not connected
G10	LA03_N	N/C	Not connected
G11	GND	GND	Ground
G12	LA08_P	N/C	Not connected
G13	LA08_N	N/C	Not connected
G14	GND	GND	Ground
G15	LA12_P	MCIOA_I2C_SCL	I2C clock for MCIO Channel A
G16	LA12_N	MCIOA_I2C_SDA	I2C data for MCIO Channel A
G17	GND	GND	Ground
G18	LA16_P	N/C	Not connected

G19	LA16_N	N/C	Not connected
G20	GND	GND	Ground
G21	LA20_P	N/C	Not connected
G22	LA20_N	N/C	Not connected
G23	GND	GND	Ground
G24	LA22_P	N/C	Not connected
G25	LA22_N	N/C	Not connected
G26	GND	GND	Ground
G27	LA25_P	N/C	Not connected
G28	LA25_N	N/C	Not connected
G29	GND	GND	Ground
G30	LA29_P	N/C	Not connected
G31	LA29_N	N/C	Not connected
G32	GND	GND	Ground
G33	LA31_P	N/C	Not connected
G34	LA31_N	N/C	Not connected
G35	GND	GND	Ground
G36	LA33_P	N/C	Not connected
G37	LA33_N	N/C	Not connected
G38	GND	GND	Ground
G39	VADJ_3	VADJ	I/O Supply Voltage
G40	GND	GND	Ground
H1	VREF_A_M2C	N/C	Not used

H2	PRSNT_M2C_L	GND	Ground
H3	GND	GND	Ground
H4	CLK0_M2C_P	N/C	Not used
H5	CLK0_M2C_N	N/C	Not used
H6	GND	GND	Ground
H7	LA02_P	N/C	Not connected
H8	LA02_N	N/C	Not connected
H9	GND	GND	Ground
H10	LA04_P	PERSTA_N_T	PCIe reset for MCIOB (active LOW)
H11	LA04_N	CPRSNTA_N_T	PCIe detect for MCIOB
H12	GND	GND	Ground
H13	LA07_P	N/C	Not used
H14	LA07_N	N/C	Not used
H15	GND	GND	Ground
H16	LA11_P	MCIOB_I2C_SCL	I2C clock for MCIO Channel B
H17	LA11_N	MCIOB_I2C_SDA	I2C data for MCIO Channel B
H18	GND	GND	Ground
H19	LA15_P	RDRV_I2C_SCL	I2C clock for Redrivers
H20	LA15_N	RDRV_I2C_SDA	I2C data for Redrivers

H21	GND	GND	Ground
H22	LA19_P	N/C	Not connected
H23	LA19_N	N/C	Not connected
H24	GND	GND	Ground
H25	LA21_P	N/C	Not connected
H26	LA21_N	N/C	Not connected
H27	GND	GND	Ground
H28	LA24_P	N/C	Not connected
H29	LA24_N	N/C	Not connected
H30	GND	GND	Ground
H31	LA28_P	N/C	Not connected
H32	LA28_N	N/C	Not connected
H33	GND	GND	Ground
H34	LA30_P	N/C	Not connected
H35	LA30_N	N/C	Not connected
H36	GND	GND	Ground
H37	LA32_P	N/C	Not connected
H38	LA32_N	N/C	Not connected
H39	GND	GND	Ground
H40	VADJ_4	VADJ	I/O Supply Voltage

Rows E,F,J and K of the HPC connector were left out of the above table. On the mezzanine card, these rows are left unconnected, with the exception of the ground and VADJ pins which are connected appropriately.

Specifications

Recommended Operating Conditions

SUPPLY VOLTAGE	MIN	TYP	MAX	UNIT
12 VDC	+11.4	+12	+12.6	V
3.3 VDC	+3.14	+3.3	+3.46	V
VADJ (1.2VDC)	+1.14	+1.2	+1.26	V
VADJ (1.5VDC)	+1.425	+1.5	+1.575	V
VADJ (1.8VDC)	+1.71	+1.8	+1.89	V
VADJ (2.5VDC)	+2.375	+2.5	+2.625	V
VADJ (3.3VDC)	+3.135	+3.3	+3.465	V

Notes:

- The mezzanine card does not use or draw any current from the 12VDC supply of the FMC carrier.
- All VADJ pins must be supplied with the same voltage chosen from one of the following levels: +1.2VDC, +1.5VDC, +1.8VDC, +2.5VDC, +3.3VDC. Note that many carriers have a system controller that will make this choice for you.

Power Consumption

> This section is incomplete and awaiting test results.

The specifications below refer to the total current draw on each of the power supplies while the MCIO PCIe FMC is connected to a development board and has 2x SSDs connected.

SUPPLY	UTILIZATION	MIN	TYP	MAX	UNIT

12 VDC		0	mA
3.3 VDC	LIGHT	TBD	mA
3.3 VDC	MAXIMUM	TBD	mA
VADJ	LIGHT	TBD	mA
VADJ	MAXIMUM	TBD	mA

- Tests performed at ambient temperature of 25 degrees C
- Tests performed using the ZCU102 development board
- Tests performed between 2x MCIO PCIe FMCs, with one in host mode and the other in device mode
- Light utilization test: FMC powered but no gigabit links enabled
- Maximum utilization test: FMC powered and 8-lane IBERT connection at 16Gbps per lane
- VADJ current draw was measured for VADJ of 1.8VDC and may be different for other levels

Note that the MCIO PCIe FMC example design will also produce an increase in power consumption of the FPGA/MPSoC on the development board due to the use of FPGA and hardware resources.

Thermal Information

We have not performed comprehensive thermal testing on the MCIO PCIe FMC, however we recommend that it be operated under ambient temperatures limited to between -20 and 70 degrees C. The active devices on the mezzanine card itself have operating ranges that exceed this recommendation and are listed in the table below.

Component Ambient Operating Temperatures

DEVICE	MIN	MAX	UNIT
TI, I2C Level Translator, TCA9416DDFR	-40	125	C

TI, 480Mbps MUX/DEMUX Switch, TMUXHS221NKGR	-40	125	C
TI, PCIe Gen5 Redriver, DS320PR810NJXT	-40	85	C
TI, Level Translator, SN74AVC4T245RSVR	-40	85	C
MicroChip, 2x Output PCIe Clock Generator, DSC557-0334FI1	-40	85	C
Microchip, 2Kbit EEPROM, 34AA02T-I/OT	-40	85	C
Amphenol ICC, 8xMCIO Connector, G97R22312HR	-40	85	C

Components that are not listed in the table above (such as resistors, capacitors) are selected to have minimum operating temperature that is lower than -20 degrees C, and maximum operating temperature that is at least 85 degrees C.

I2C (EEPROM) Timing

The serial EEPROM (part number Microchip, 2Kbit EEPROM, 34AA02T-I/OT) has a maximum operating clock frequency of 400 kHz.

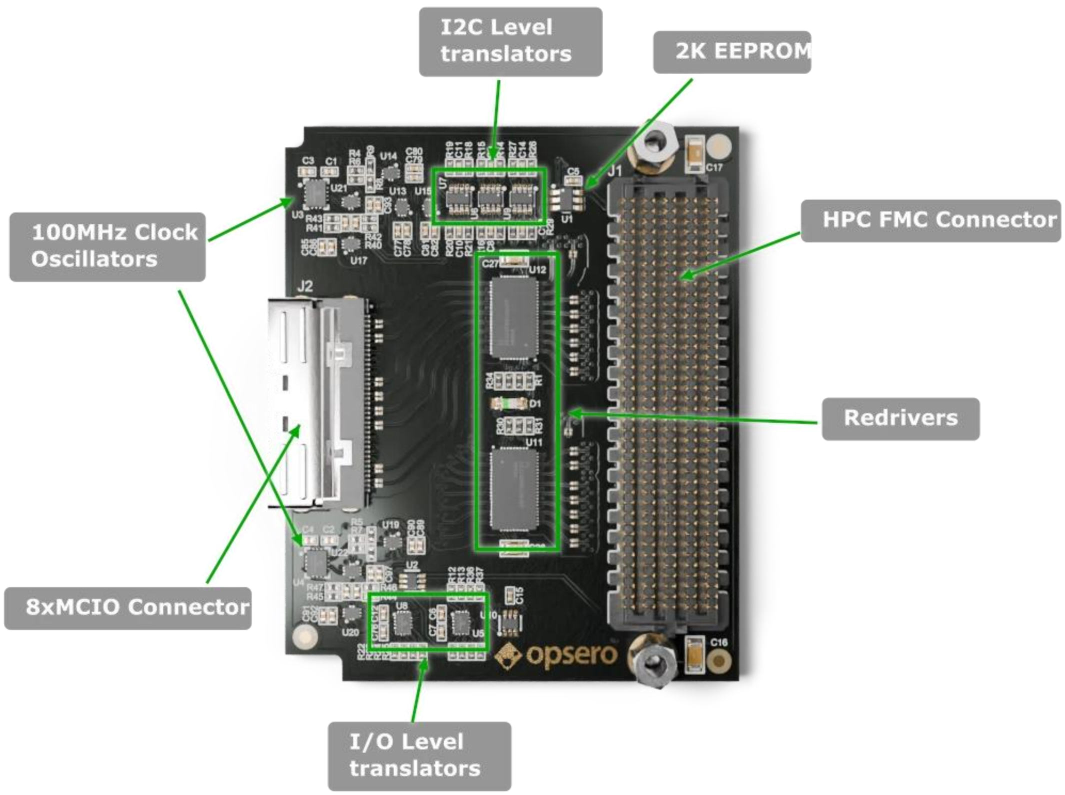
Certifications

- RoHS
- CE
- UKCA

Detailed Description

Hardware Overview

The figure below illustrates the various hardware components that are located on the top-side of the MCIO PCIe FMC.



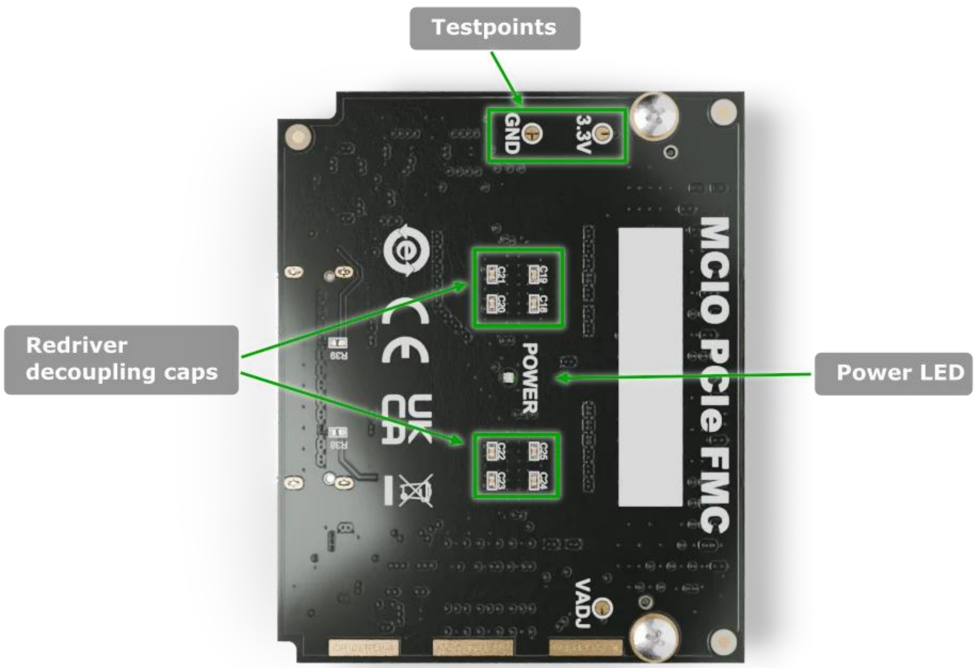
MCIO PCIe FMC labelled top-side

The main components on the top-side of the mezzanine card are:

- 8xMCIO Connector
- High Pin Count FMC Connector
- 2K EEPROM
- 2x 100MHz Clock oscillators
- 2x PCIe Redrivers

- Level translators

The figure below illustrates the various hardware components that are located on the bottom-side of the mezzanine card.



MCIO PCIe FMC labelled bottom-side

The main components on the bottom-side of the mezzanine card are:

- FMC Power indicator LED
- Redriver decoupling capacitors
- Test points for power supplies

MCIO connector

The Amphenol ICC, 8xMCIO Connector, [G97R22312HR](G97R22312HR), has 8 gigabit transceiver lanes that can be used as two 4-lane links, or as a single 8-lane link. Although the connector and mezzanine card are optimized for PCIe links, they can be used with other serial link standards.

The MCIO connector carries two types of signals: transceiver lanes and sideband signals. Both are organized into two independent channels, A and B.

The transceiver lanes handle high-speed serial data and are labelled PER (receive) and PET (transmit). Lanes 0 through 3 belong to channel A, and lanes 4 through 7 belong to channel B.

Each channel also has its own set of sideband signals, identified by an A or B suffix:

- REFCLKA/B_P/N — Reference clock
- PERSTA/B_N — PCIe reset
- PRSNTA/B_N — Device present detect
- 2WA/B_SCL and 2WA/B_SDA — I2C clock and data
- BP_TYPEA/B — Backplane type (not used on this mezzanine card)
- CWAKEA/B_N — Clock wake (not used on this mezzanine card)

The pinout of the sideband signals on the MCIO connector depends on whether it is being used in host or device mode and is determined by a logic signal on the FMC interface. This allows the same connector to operate in both host mode and device mode, with the carrier board's FPGA selecting the desired mode on configuration.

The pinout of the MCIO connector in each mode is shown in the table below:

Pin #	Host mode	Device mode	Pin #	Host mode	Device mode
A1	GND	GND	B1	GND	GND
A2	PER_0P	PER_0P	B2	PET_0P	PET_0P
A3	PER_0N	PER_0N	B3	PET_0N	PET_0N
A4	GND	GND	B4	GND	GND
A5	PER_1P	PER_1P	B5	PET_1P	PET_1P
A6	PER_1N	PER_1N	B6	PET_1N	PET_1N
A7	GND	GND	B7	GND	GND
A8	BP_TYPEA	2WA_SCL	B8	2WA_SCL	BP_TYPEA

A9	CWAKEA_N	2WA_SDA	B9	2WA_SDA	CWAKEA_N
A10	GND	GND	B10	GND	GND
A11	REFCLKA_P	PERSTA_N	B11	PERSTA_N	REFCLKA_P
A12	REFCLKA_N	PRSNTA_N	B12	PRSNTA_N	REFCLKA_N
A13	GND	GND	B13	GND	GND
A14	PER_2P	PER_2P	B14	PET_2P	PET_2P
A15	PER_2N	PER_2N	B15	PET_2N	PET_2N
A16	GND	GND	B16	GND	GND
A17	PER_3P	PER_3P	B17	PET_3P	PET_3P
A18	PER_3N	PER_3N	B18	PET_3N	PET_3N
A19	GND	GND	B19	GND	GND
A20	PER_4P	PER_4P	B20	PET_4P	PET_4P
A21	PER_4N	PER_4N	B21	PET_4N	PET_4N
A22	GND	GND	B22	GND	GND
A23	PER_5P	PER_5P	B23	PET_5P	PET_5P
A24	PER_5N	PER_5N	B24	PET_5N	PET_5N
A25	GND	GND	B25	GND	GND
A26	BP_TYPEB	2WB_SCL	B26	2WB_SCL	BP_TYPEB
A27	CWAKEB_N	2WB_SDA	B27	2WB_SDA	CWAKEB_N
A28	GND	GND	B28	GND	GND
A29	REFCLKB_P	PERSTB_N	B29	PERSTB_N	REFCLKB_P
A30	REFCLKB_N	PRSNTB_N	B30	PRSNTB_N	REFCLKB_N
A31	GND	GND	B31	GND	GND

A32	PER_6P	PER_6P	B32	PET_6P	PET_6P
A33	PER_6N	PER_6N	B33	PET_6N	PET_6N
A34	GND	GND	B34	GND	GND
A35	PER_7P	PER_7P	B35	PET_7P	PET_7P
A36	PER_7N	PER_7N	B36	PET_7N	PET_7N
A37	GND	GND	B37	GND	GND

The MCIO connector organizes its pins into two rows: the A-side and the B-side. The high-speed differential pairs are arranged such that the receive pairs (PER) are on the A-side and the transmit pairs (PET) are on the B-side. These assignments are consistent regardless of whether the connector is operating in host or device mode — the data lanes themselves do not change function between modes.

When an MCIO cable connects two devices, it crosses the A-side of one connector to the B-side of the other, and vice versa. This crossover is what establishes the correct TX-to-RX routing required by PCIe: the transmit pairs (PET) from one end of the cable arrive at the receive pairs (PER) of the other end, and the same applies in the opposite direction. No additional switching of the high-speed data lanes is needed.

However, the cable crossover also affects the sideband signals that occupy specific pin positions alongside the data lanes. In a standard PCIe connection, certain sideband signals are outputs on the host side and inputs on the device side. For example, the reference clock (REFCLK) is provided by the host, while the reset signal (PERST_N) is driven by the host toward the device. The presence detect (PRSNT_N) signal, on the other hand, is driven by the device toward the host. Because the cable swaps A-side and B-side pins, these sideband signals naturally land on the correct pins at each end — but only if the connector is wired for the appropriate mode.

Since the MCIO PCIe FMC supports both host and device modes through the same connector, the sideband pins must serve a dual purpose. In host mode, the A-side sideband pins carry host-sourced signals such as REFCLK and the B-side carries device-sourced signals such as PERST_N and PRSNT_N. In device mode, these roles are reversed to match what the remote host expects to see at the other end of the cable. The mezzanine card manages this by using multiplexers on the sideband pins, controlled by a mode selection logic signal on the FMC interface, which routes the correct signals to the correct pins based on the selected operating mode.

High-speed Switches

The mezzanine card uses several high-speed switches (TI, 480Mbps MUX/DEMUX Switch, TMUXHS221NKGR) to allow the sideband signals to be switched between **host** and **device** mode. Each switch determines the purpose of a single sideband pair. For example, pair A11/A12 connects to clock oscillator output in host mode, while in device mode it connects to PERSTA_N and CPRSNTA_N. The SEL input of all switches is connected to the HOST_MODE_N signal that is driven by the FPGA.

EEPROM

The EEPROM (Microchip, 2Kbit EEPROM, 34AA02T-I/OT) stores IPMI FRU data that can be read by the carrier board and contains the following information:

- Manufacturer name (Opsero Electronic Design Inc.)
- Product name
- Product part number
- Serial number
- Power supply requirements

The FRU data is read by some carrier boards to determine the correct VADJ voltage to apply to the mezzanine card. All Opsero FMC products have their EEPROMs programmed with valid FRU data to allow these carrier boards to correctly power them.

> Erasing or writing over the contents of the EEPROM can corrupt the IPMI FRU data making the mezzanine card unusable with carrier boards that require the information. We recommend that you do not use the mezzanine card's EEPROM for non-volatile storage but instead use the storage options provided by the carrier board. If you mistakenly erase or corrupt the contents of the EEPROM, you can reprogram it using the Opsero FMC EEPROM Tool. For more information, see: FMC EEPROM tool.

High Pin Count FMC Connector

The MCIO PCIe FMC has a high pin count (HPC) FMC (FPGA Mezzanine Card) connector for interfacing with an FPGA or SoC development board. The part number of this connector is Samtec, High pin count FMC connector, Module side, ASP-134488-01. This HPC FMC connector can be mated with LPC, HPC or FMC+ carrier connectors.

Note: When mated with an LPC FMC connector, only one gigabit transceiver is connected. To get full functionality from the mezzanine card, it is recommended to use it with fully connected HPC or FMC+ connectors.

The pinout of this connector conforms to the VITA 57.1 FPGA Mezzanine Card Standard (for more information, see Pin configuration. For more information on the FMC connector and the VITA 57.1 standard, see the Samtec page on VITA 57.1.

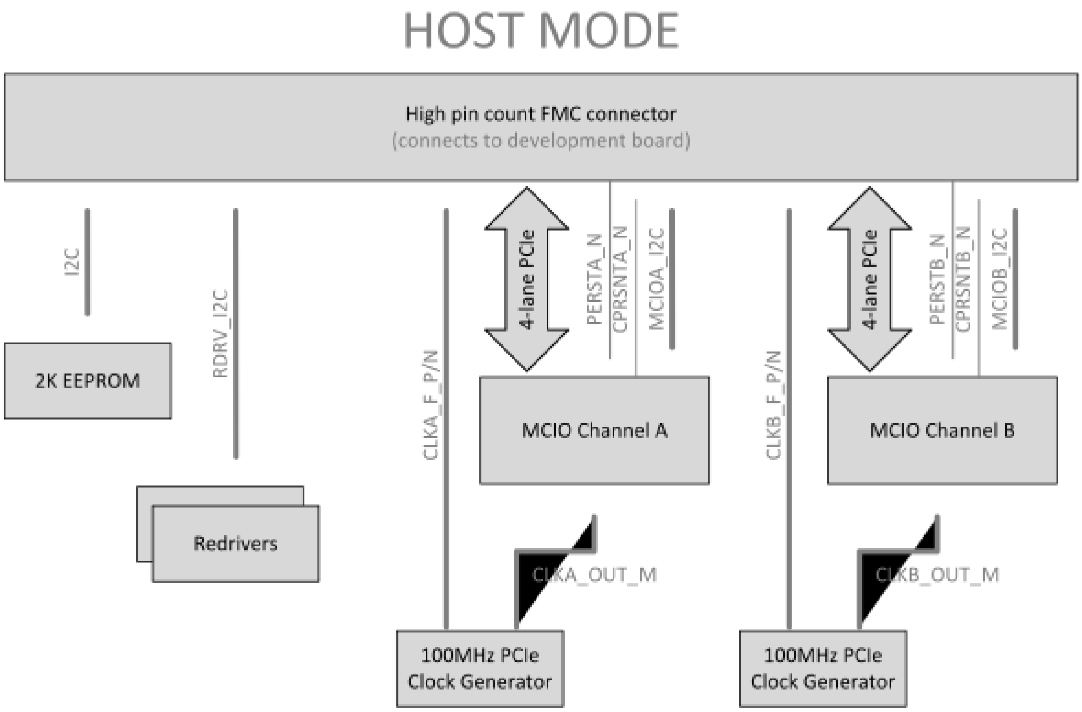
I/O Interfaces

The FMC connector provides power to the MCIO PCIe FMC and also presents the following I/O signals to the FPGA fabric of the development board:

- 8x gigabit transceivers
- PERSTA_N and PERSTB_N active-low reset signals for channel A and B (driven by FPGA in host mode, driven by MCIO in device mode)
- PRSNTA_N and PRSNTB_N active-low present signals for channel A and B (driven by MCIO in host mode, driven by FPGA in device mode)
- SBA_DISABLE and SBB_DISABLE active-high signals to disable sidebands for channel A and B
- HOST_MODE_N for selecting between host and device modes
- LOCAL_CLKS_N for selecting the FPGA clock source between local clock and MCIO clock (in device mode only)
- 2x LVDS 100MHz reference clocks
- I2C for FMC EEPROM
- I2C for MCIO Channel-A
- I2C for MCIO Channel-B
- I2C for Redriver configuration

Host Mode

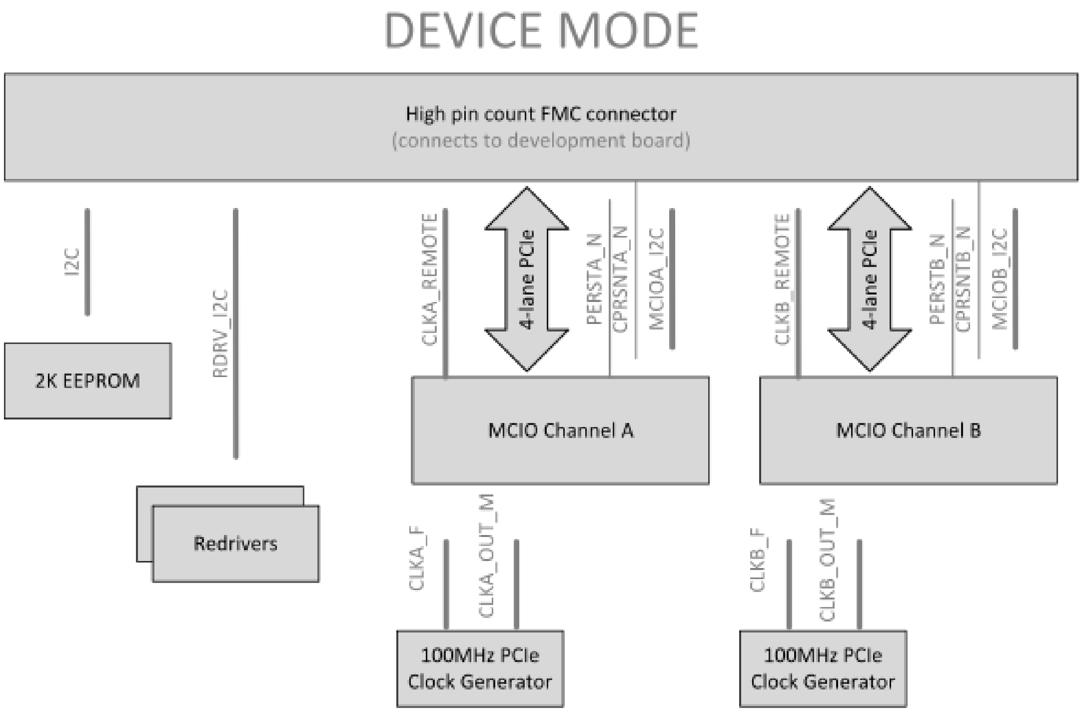
The figure below illustrates the main connections to the FMC connector in host mode (HOST_MODE_N = LOW, LOCAL_CLKS_N = LOW). For clarity we have left out the switches and level translators from the diagram.



FMC Connector

Device Mode

The figure below illustrates the main connections to the FMC connector in device mode (HOST_MODE_N = HIGH, LOCAL_CLKS_N = HIGH). For clarity we have left out the switches and level translators from the diagram.



FMC Connector

Gigabit Transceivers

The 8x PCIe lanes of the MCIO connector are routed to FMC pins that are dedicated to gigabit transceivers. The first four lanes are referred to as channel A, while the second four lanes are referred to as channel B (not to be confused with row-A and row-B of the MCIO connector). The connections are shown in the tables below.

MCIO Channel A

Direction	PCIe lane	FMC Pin	FMC name	Net name
MCIO-to-FPGA	0	C6/C7	DP0_M2C_P/N	PERA_0_P/N
	1	A2/A3	DP1_M2C_P/N	PERA_1_P/N
	2	A6/A7	DP2_M2C_P/N	PERA_2_P/N
	3	A10/A11	DP3_M2C_P/N	PERA_3_P/N
FPGA-to-MCIO	0	C2/C3	DP0_C2M_P/N	PETA_0_P/N

	1	A22/A23	DP1_C2M_P/N	PETA_1_P/N
	2	A26/A27	DP2_C2M_P/N	PETA_2_P/N
	3	A30/A31	DP3_C2M_P/N	PETA_3_P/N

MCIO Channel B

Direction	PCIe lane	FMC Pin	FMC name	Net name
MCIO-to-FPGA	0	A14/A15	DP4_M2C_P/N	PERB_0_P/N
	1	A18/A19	DP5_M2C_P/N	PERB_1_P/N
	2	B16/B17	DP6_M2C_P/N	PERB_2_P/N
	3	B12/B13	DP7_M2C_P/N	PERB_3_P/N
FPGA-to-MCIO	0	A34/A35	DP4_C2M_P/N	PETB_0_P/N
	1	A38/A39	DP5_C2M_P/N	PETB_1_P/N
	2	B36/B37	DP6_C2M_P/N	PETB_2_P/N
	3	B32/B33	DP7_C2M_P/N	PETB_3_P/N

Reference clocks

The mezzanine card has two clock oscillators (MicroChip, 2x Output PCIe Clock Generator, DSC557-0334FI1), one for each MCIO channel. Each clock oscillator generates two synchronous 100MHz clocks; one LVDS and the other HCSL. The LVDS clocks are intended for driving the GT ref clocks, while the HCSL clocks are intended for the MCIO.

The GT ref clocks can be driven either by the on-board clock oscillators (locally) or by the remote clocks supplied by the connected MCIO host (when used in device mode). The clocks are selected by driving the LOCAL_CLKS_N signal (see below for more information on this signal).

Synchronous to	FMC Pin	FMC name	Net name
MCIO Channel A	D4/D5	GBTCLK0_M2C_P/N	CLKA_F_P/N
MCIO Channel B	B20/B21	GBTCLK1_M2C_P/N	CLKB_F_P/N

When used in host mode, the GT ref clocks **must be driven** with the local clocks (LOCAL_CLKS_N = LOW). When used in device mode, it is typical to use the remote clock provided by the connected MCIO host to drive the GT ref clocks (LOCAL_CLKS_N = HIGH).

PERST_N

The PERSTA_N and PERSTB_N signals are active-low reset signals for MCIO channels A and B respectively. They are driven by the FPGA in host mode, and driven by the MCIO link partner in device mode. Level translators convert these signals from VADJ levels (FPGA side) to 3.3V levels (MCIO side). The function of these signals is shown in the table below:

PERSTA/B_N	Function
0 (LOW)	MCIO device in reset
1 (HIGH)	MCIO device operational

Pull-up resistors are tied to these signals on the mezzanine card on the 3.3V side so that they are not left floating if in device mode and the MCIO cable is disconnected.

Pull-up resistors are tied to these signals on the mezzanine card on the VADJ side so that they are not left floating if in host mode and the pins have not been connected in the FPGA design.

PRSNT_N

The PRSNTA_N and PRSNTB_N signals are active-low signals driven by the MCIO device to indicate presence. In host mode, the FPGA can read this signal to determine if an MCIO device is connected. In device mode, the FPGA should drive this signal LOW to indicate its presence to the MCIO host. The functionality of these signals is described in the table below:

PEDETA/B_N	Function
0 (LOW)	Device present
1 (HIGH)	Device NOT present

Pull-up resistors are tied to these signals on the mezzanine card so that they default to HIGH when in host mode and the MCIO cable is disconnected.

Pull-down resistors are tied to these signals on the mezzanine card on the VADJ side so that they are not left floating if in device mode and the pins have not been connected in the FPGA design.

HOST_MODE_N

The HOST_MODE_N signal is an active-low signal that determines whether the mezzanine card is in host or device mode. When driven LOW, the mezzanine card is configured for host mode. When driven HIGH, the mezzanine card is configured for device mode.

HOST_MODE_N	Function
0 (LOW)	Host mode
1 (HIGH)	Device mode

LOCAL_CLKS_N

The LOCAL_CLKS_N signal is an active-low signal that determines whether the gigabit transceiver reference clocks will be driven by local or remote clock sources. When used in device mode, we can choose to drive the GT ref clocks with the local clocks generated by the mezzanine card's 100MHz clock oscillators, or with the remote clocks provided by the connected MCIO host.

When driven LOW, the local clock oscillators will drive the GT reference clock inputs. When driven HIGH, the MCIO host provided clocks will drive the GT reference clock inputs. Note that when used in host mode, the local clock oscillators should *always* be used as the GT reference clocks and LOCAL_CLK_N should always be driven LOW.

LOCAL_CLKS_N	Function
0 (LOW)	Local clocks drive GT refclks
1 (HIGH)	Remote clocks (from MCIO host) drive GT refclks

SBx_DISABLE

The SBA_DISABLE and SBB_DISABLE signals can be used to disable the sideband signals of MCIO channel A and B respectively. The main purpose of this feature is to allow support of the Open Compute Project M-XIO standard. For most other applications of this mezzanine card, both sideband channels should be enabled.

The MCIOx8 connector on the mezzanine card is wired for SFF-9402 standard by default. To make the connector compatible with OCP M-XIO standard, albeit without 3P3VAUX_MGMT, USB or FLEXIO support, drive the SBB_DISABLE signal HIGH to disconnect the sideband B signals.

Disabling the sideband signals of a channel leaves those MCIO pins in a high-impedance state.

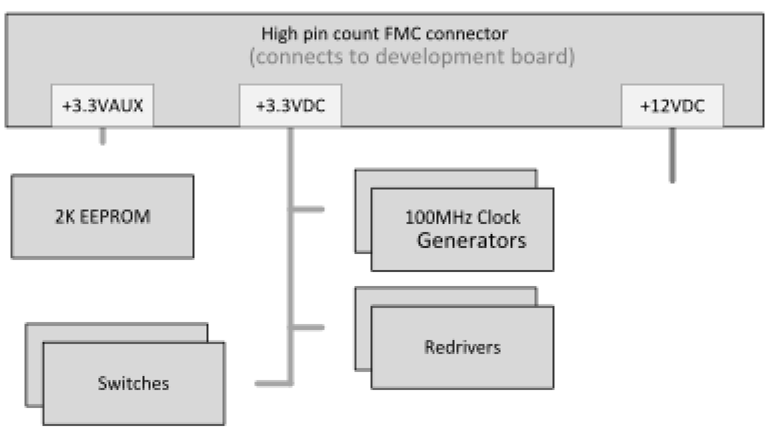
SBA/B_DISABLE	Function
0 (LOW)	Enable sideband signals
1 (HIGH)	Disable sideband signals

Power Supplies

All power required by the MCIO PCIe FMC is supplied by the development board through the FMC connector:

- +12VDC (not used by the mezzanine card)
- +3.3VDC
- +3.3VAUX (for powering EEPROM only)
- VADJ: +1.2VDC-3.3VDC

All devices on the mezzanine card are powered by the 3.3VDC supply of the FMC connector. The +12VDC supply of the FMC connector is not used by this mezzanine card. The VADJ supply does not power any devices but is used to provide reference to the level translators.



Power supplies

The 3.3VDC Supply

The 3.3VDC supply provides power for the redrivers, the clock oscillators, the switches, the inverters, the EEPROM and the level translators.

VADJ Supply

The adjustable voltage supply (VADJ), is the I/O voltage that is supplied by all standard FMC carriers. The MCIO PCIe FMC can accept any VADJ voltage in the range of 1.2V to 3.3V. The mezzanine card has an onboard FRU EEPROM that specifies acceptance of any VADJ voltage within the range 1.2V to 3.3V (see note below). All carriers with a power management system will read this EEPROM on power-up and apply a voltage in the range specified by the EEPROM. Note that some development boards require the VADJ voltage to be configured by a DIP switch or jumper placement, in which case we suggest that it be set to 1.8V.

Power LED and testpoints

A single green LED on the mezzanine card is used to indicate when the required power supplies are active. The location of this LED can be seen in the labelled bottom view of the board above. The LED indicates when the FMC's 12VDC, 3.3VDC and VADJ voltages are active.

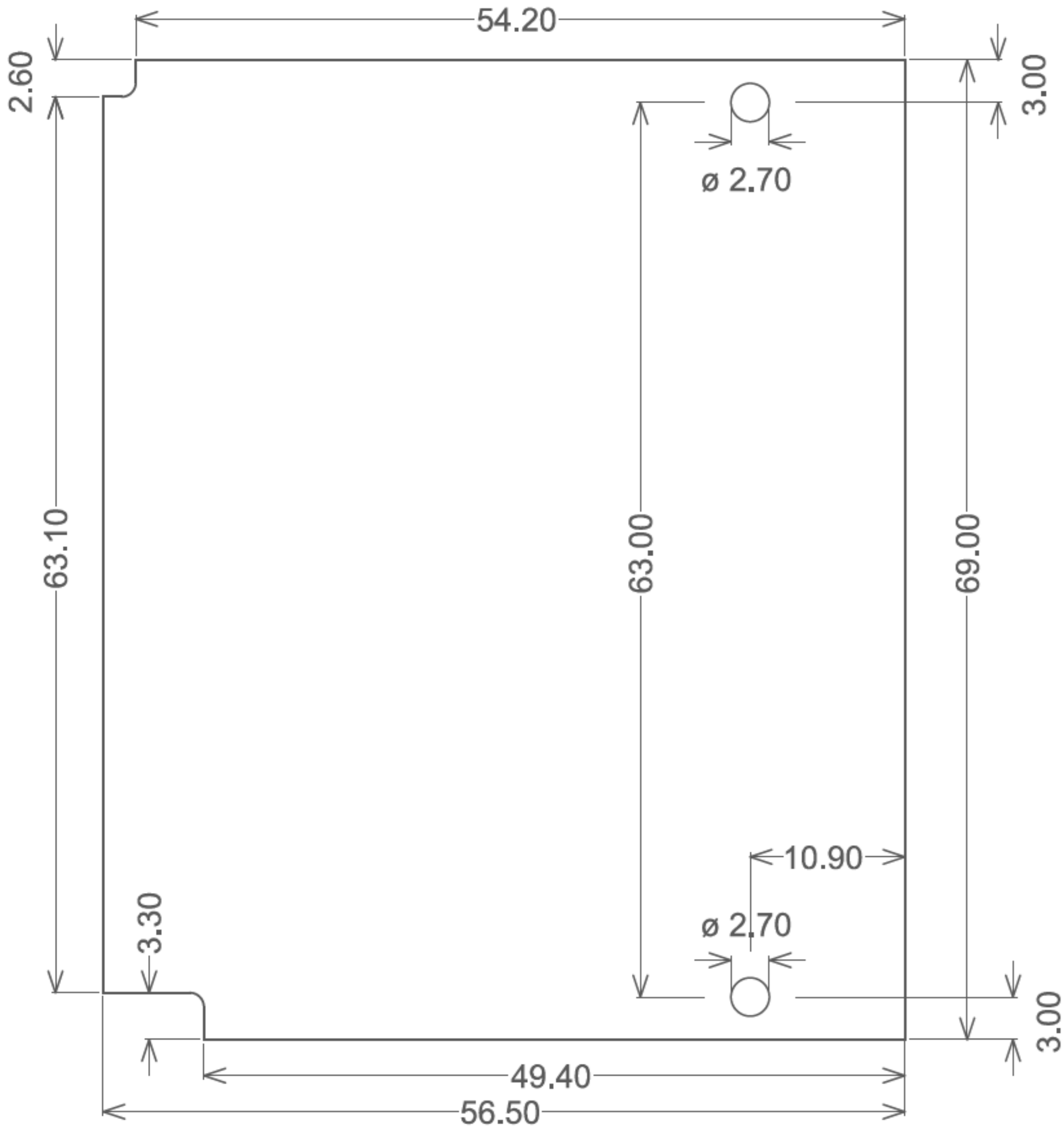
To aid hardware debug, test points are accessible on the bottom side of the mezzanine card for the 3.3V and VADJ power supplies of the MCIO PCIe FMC.

Mechanical Information

Dimensions

The mechanical dimensions of the MCIO PCIe FMC are illustrated in the figures below. All dimensions are in millimeters (mm).

The assembly drawings are also available as PDF files that you can download at the provided links.



MCIO PCIe FMC mechanical drawing

- [MCIO PCIe FMC Rev-A Assembly Drawing PDF]

The 3D Model

The 3D model of the board is available as a STEP file at the link below:

- [MCIO PCIe FMC Rev-A 3D STEP model]

Mezzanine fastening hardware

For mechanical fastening of the mezzanine card to the carrier board, the MCIO PCIe FMC comes with 2x hex standoffs. We **highly recommend** using machine screws on each of these standoffs to fix the mezzanine card to the carrier board.

The hex standoff and machine screw part numbers are listed below:

- Hex standoff, Thread M2.5 x 0.45, Brass, Board-to-board length 10mm **Part number:** V6516C **Manufacturer:** Assmann
- Machine screw, Thread M2.5 x 0.45, Length (below head) 4mm, Stainless steel, Phillips head **Part number:** 90116A105 **Supplier:** McMaster-Carr

Compatible Boards

The following development boards are compatible with the MCIO PCIe FMC and can support at least one channel of the 8xMCIO connector. If you know of a board that is not listed here and you would like to know if it is compatible, please contact us.

Note that we don't currently have example designs for all of these carrier boards. For a list of carrier boards for which we do have example designs, please refer to the list of supported carriers in the reference design documentation.

Series-7 boards

Carrier	FMC	Ref design	PCIe	MCIO Ch-A	MCIO Ch-B
AMD Xilinx KC705 Kintex-7 Development board	HPC	Coming soon	Gen2	4-lanes	Not supported
AMD Xilinx KC705 Kintex-7 Development board	LPC	Coming soon	Gen2	1-lane [2]	Not supported [2]

AMD Xilinx VC707 Virtex-7 Development board	HPC1	Coming soon	Gen2	4-lanes	4-lanes
AMD Xilinx VC707 Virtex-7 Development board	HPC2	Coming soon	Gen2	4-lanes	4-lanes
AMD Xilinx VC709 Virtex-7 Development board	HPC	Coming soon	Gen3	4-lanes	4-lanes
AMD Xilinx ZC706 Zynq-7000 Development board	HPC	Coming soon	Gen2	4-lanes	Not supported [1]
AMD Xilinx ZC706 Zynq-7000 Development board	LPC	Coming soon	Gen2	1-lane [2]	Not supported [2]
Avnet PicoZed FMC Carrier Card V2 Zynq-7000	LPC	Coming soon	Gen2	1-lane [2]	Not supported [2]

Development
Board

UltraScale boards

Carrier	FMC	Ref design	PCIe	MCIO Ch-A	MCIO Ch-B
AMD Xilinx KCU105 Kintex UltraScale Development board	HPC	Coming soon	Gen3	4-lanes	4-lanes
AMD Xilinx KCU105 Kintex UltraScale Development board	LPC	Coming soon	Gen3	1-lane [2]	Not supported [2]
AMD Xilinx VCU108 Virtex UltraScale Development board	HPC0	✗	Gen3	4-lanes	4-lanes
AMD Xilinx VCU108 Virtex UltraScale Development board	HPC1	✗	Gen3	4-lanes	4-lanes

Zynq Ultrascale+ boards

Carrier	FMC	Ref design	PCIe	MCIO Ch-A	MCIO Ch-B
AMD Xilinx ZCU104 Zynq UltraScale+ Development board	LPC	Coming soon	Gen3	1-lane [2]	Not supported [2]
AMD Xilinx ZCU102 Zynq UltraScale+ Development board	HPC0	✗	Gen3	4-lanes [3]	4-lanes [3]
AMD Xilinx ZCU102 Zynq UltraScale+ Development board	HPC1	✗	Gen3	4-lanes [3]	4-lanes [3]
AMD Xilinx ZCU106 Zynq UltraScale+ Development board	HPC0	Coming soon	Gen3	4-lanes	4-lanes
AMD Xilinx ZCU106 Zynq	HPC1	Coming soon	Gen3	1-lanes	Not supported

UltraScale+ Development board					
AMD Xilinx ZCU111 Zynq UltraScale+ Development board	FMC+	Coming soon	Gen3	4-lanes	4-lanes
AMD Xilinx ZCU208 Zynq UltraScale+ Development board	FMC+	Coming soon	Gen3	4-lanes	4-lanes
Avnet UltraZed EV Carrier Zynq UltraScale+ Development board	HPC	Coming soon	Gen3	4-lanes	4-lanes
Trenz UltraITX+ Baseboard Zynq UltraScale+ Development board	HPC	✗	Gen3	4-lanes [3]	4-lanes [3]

Ultrascale+ boards

Carrier	FMC	Ref design	PCIe	MCIO Ch-A	MCIO Ch-B

AMD Xilinx VCU118 Virtex UltraScale+ Development board	HPC	✗	Gen3	Not supported	Not supported
AMD Xilinx VCU118 Virtex UltraScale+ Development board	FMC+	Coming soon	Gen3	4-lanes	4-lanes

Versal boards

Carrier	FMC	Ref design	PCIe	MCIO Ch-A	MCIO Ch-B
AMD Xilinx VCK190 Versal AI Core Development board	FMC+1	Coming soon	Gen4	4-lanes	4-lanes
AMD Xilinx VCK190 Versal AI Core Development board	FMC+2	Coming soon	Gen4	4-lanes	4-lanes
AMD Xilinx VEK280 Versal AI	FMC+	Coming soon	Gen4	4-lanes	4-lanes

Edge Development board					
AMD Xilinx [VHK158](#) Versal HBM Series Development board	FMC+	Coming soon	Gen4	4-lanes	Not supported [4]
AMD Xilinx [VMK180](#) Versal Prime Series Development board	FMC+1	Coming soon	Gen4	4-lanes	4-lanes
AMD Xilinx [VMK180](#) Versal Prime Series Development board	FMC+2	Coming soon	Gen4	4-lanes	4-lanes
AMD Xilinx [VPK120](#) Versal Premium Series Development board	FMC+	Coming soon	Gen4	4-lanes	Not supported [4]
AMD Xilinx [VPK180](#)	FMC+	Coming soon	Gen4	4-lanes	Not supported [4]

Versal
Premium
Series
Development
board

Compatibility requirements

If you need to determine the compatibility of a development board that is not listed here, or you are designing a carrier board to mate with the MCIO PCIe FMC, you can check your board against the list of requirements below.

VADJ

The carrier board must have the ability to supply a VADJ voltage between 1.2VDC and 3.3VDC.

Gigabit transceivers

The FPGA or MPSoC device must have gigabit transceivers and they must be routed to the FMC connector. For support of both MCIO channels, transceivers DP0-DP7 must all be connected to the FPGA. In the AMD Xilinx devices, the transceivers are typically grouped into quads containing 4 transceivers. Ideally, each MCIO channel should be connected to a single quad and the lane ordering should match the MGT ordering as shown in the tables below:

Quad 1

The first quad should be connected to MCIO Channel-A as follows:

FPGA pin	PCIe lane	FMC Pin	FMC name	Net name
MGT_RXP/N0	0	C6/C7	DP0_M2C_P/N	PERA_0_P/N
MGT_TXP/N0	0	C2/C3	DP0_C2M_P/N	PETA_0_P/N
MGT_RXP/N1	1	A2/A3	DP1_M2C_P/N	PERA_1_P/N
MGT_TXP/N1	1	A22/A23	DP1_C2M_P/N	PETA_1_P/N
MGT_RXP/N2	2	A6/A7	DP2_M2C_P/N	PERA_2_P/N
MGT_TXP/N2	2	A26/A27	DP2_C2M_P/N	PETA_2_P/N
MGT_RXP/N3	3	A10/A11	DP3_M2C_P/N	PERA_3_P/N

MGT_TXP/N3	3	A30/A31	DP3_C2M_P/N	PETA_3_P/N

The clock reference for this channel (FMC pins GBTCLK0_M2C_P/N) should be connected to MGTREFCLK0P/N or MGTREFCLK1P/N of this quad.

Quad 2

The second quad should be connected to MCIO Channel-B as follows:

Direction	PCIe lane	FMC Pin	FMC name	Net name
MGT_RXP/N0	0	A14/A15	DP4_M2C_P/N	PERB_0_P/N
MGT_TXP/N0	0	A34/A35	DP4_C2M_P/N	PETB_0_P/N
MGT_RXP/N1	1	A18/A19	DP5_M2C_P/N	PERB_1_P/N
MGT_TXP/N1	1	A38/A39	DP5_C2M_P/N	PETB_1_P/N
MGT_RXP/N2	2	B16/B17	DP6_M2C_P/N	PERB_2_P/N
MGT_TXP/N2	2	B36/B37	DP6_C2M_P/N	PETB_2_P/N
MGT_RXP/N3	3	B12/B13	DP7_M2C_P/N	PERB_3_P/N
MGT_TXP/N3	3	B32/B33	DP7_C2M_P/N	PETB_3_P/N

The clock reference for this channel (FMC pins GBTCLK1_M2C_P/N) should be connected to MGTREFCLK0P/N or MGTREFCLK1P/N of this quad.

Reference clocks

The mezzanine card generates two 100MHz reference clocks and supplies them to the carrier board via pins GBTCLK0_M2C_P/N and GBTCLK1_M2C_P/N of the FMC connector. The reference clocks are intended to clock the gigabit transceivers and are standard LVDS signals as required by VITA 57.1 Rule 5.54. The gigabit transceivers in AMD Xilinx devices support LVDS reference clocks. For devices of other manufacturers, please ensure that the reference clock inputs of the gigabit transceivers can support the LVDS signaling standard.

Note on Altera devices: Some Altera devices such as the Agilex-7 have gigabit transceivers (F-Tile FGT) that do not support LVDS reference clocks. When using Altera devices, please ensure that the gigabit transceivers that are connected to the FMC/FMC+ connector of your development board actually support LVDS reference clocks. We have found that the following development boards are not compatible with MCIO PCIe FMC for this reason:

- iWave Agilex-7 SoC FPGA SOM Development Kit

Required I/O

The following I/O pins should be connected to the FPGA as they are required by the mezzanine card:

FMC Pin	FMC name	Net	Description
G6	LA00_P_CC	PERSTA_N_T	PCIe reset for MCIO Channel A (active low)
G7	LA00_N_CC	CPRSNTA_N_T	Present for MCIO Channel A (active low)
H10	LA04_P	PERSTB_N_T	PCIe reset for MCIO Channel B (active low)
H11	LA04_N	CPRSNTB_N_T	Present for MCIO Channel B (active low)
C14	LA10_P	SBA_DISABLE_T	Disable sideband A signals
C15	LA10_N	SBB_DISABLE_T	Disable sideband B signals
C18	LA14_P	HOST_MODE_N_T	Host mode enable active-low (0:HOST MODE, 1:DEVICE MODE)

C19	LA14_N	LOCAL_CLKS_N_T	Local/remote clock select (0:LOCAL, 1:REMOTE)
G15	LA12_P	MCIOA_I2C_SCL	I2C clock for MCIO Channel A
G16	LA12_N	MCIOA_I2C_SDA	I2C data for MCIO Channel A
H16	LA11_P	MCIOB_I2C_SCL	I2C clock for MCIO Channel B
H17	LA11_N	MCIOB_I2C_SDA	I2C data for MCIO Channel B
H19	LA15_P	RDRV_I2C_SCL	I2C clock for Redrivers
H20	LA15_N	RDRV_I2C_SDA	I2C data for Redrivers

Notes

[1] *Zynq-7000 devices only have 1 PCIe block*

[2] *LPC connectors can only support 1-lane PCIe*

[3] *This board's device does not have integrated PCIe blocks, but it can be used with 3rd party IP to implement the required PCIe root complex*

[4] *VHK150, VPK120 and VPK180 boards have enough PCIe blocks and GTs to support both MCIO channels, however one of the PCIe blocks is located on the opposite side of the device to the relevant GTs, making routing a challenge. For this reason we do not support the use of MCIO Channel B on these boards.*

Board Revision History

Rev A

- The MCIO PCIe FMC (OP103) is an upgrade of the original MCIO PCIe Host FMC (OP100) product which is now discontinued.
- Date of first manufacture: 2026-02-23
- Commercially released

Ordering Information

Vendor	Part name	Part number
Opsero	MCIO PCIe FMC	OP103

Revision History

Date	Version	Description
2026-04-21	1.0	Initial PDF release.

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