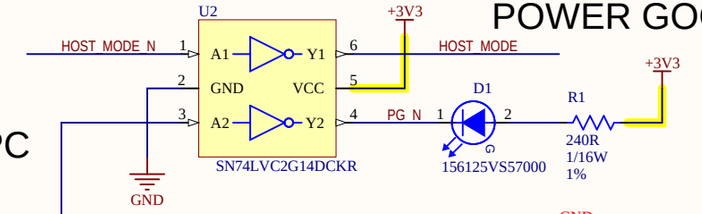
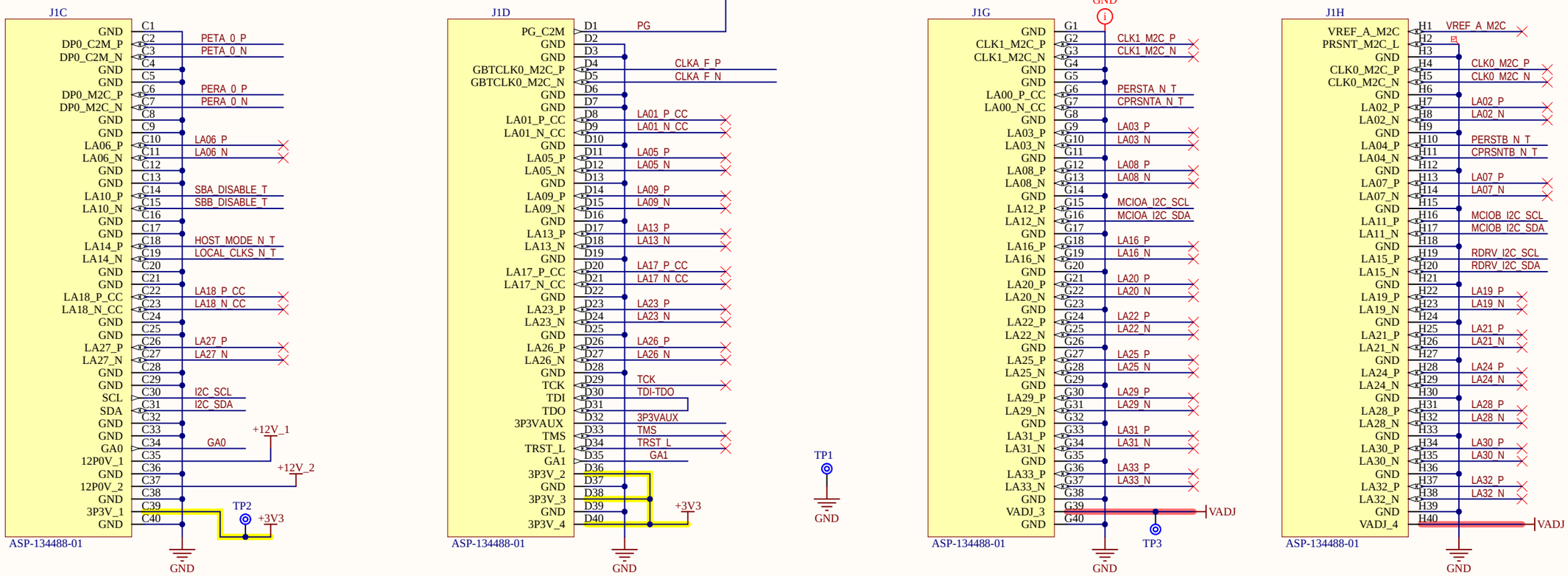
REV.	DESCRIPTION	DATE	APPROVED
A-1	First release	2026-02-03	J Johnson

POWER GOOD LED

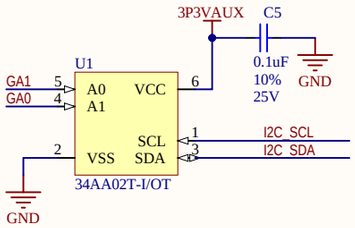


FMC PINS COMMON WITH LPC



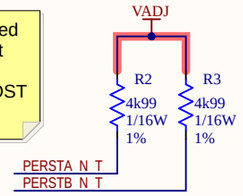
In accordance with the VITA 57.1 standard: GA0 goes to A1, GA1 goes to A0

EEPROM

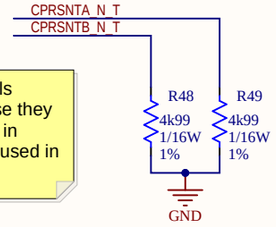


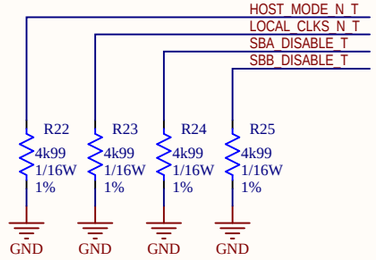
DEFAULTS

PERST_N signals pulled up in case they are not connected in FPGA design and used in HOST MODE.



CPRSNT_N signals pulled down in case they are not connected in FPGA design and used in DEVICE MODE.





HOST_MODE_N, LOCAL_CLKS_N and SBB_ENABLE signals pulled down in case not connected in FPGA design

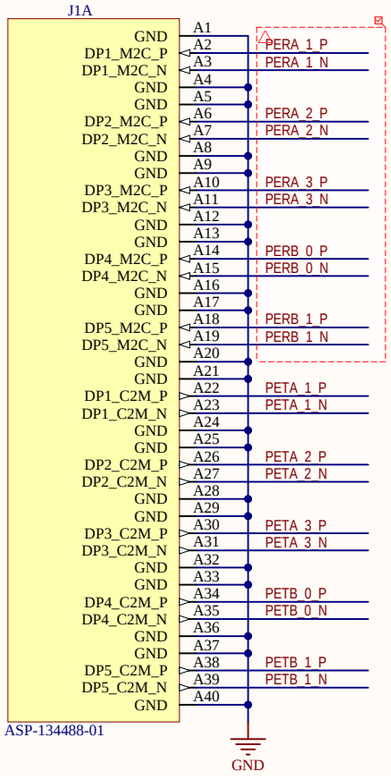
Defaults =
- HOST MODE enabled
- Use local clocks
- Sidebands A + B enabled (SFF-9402)

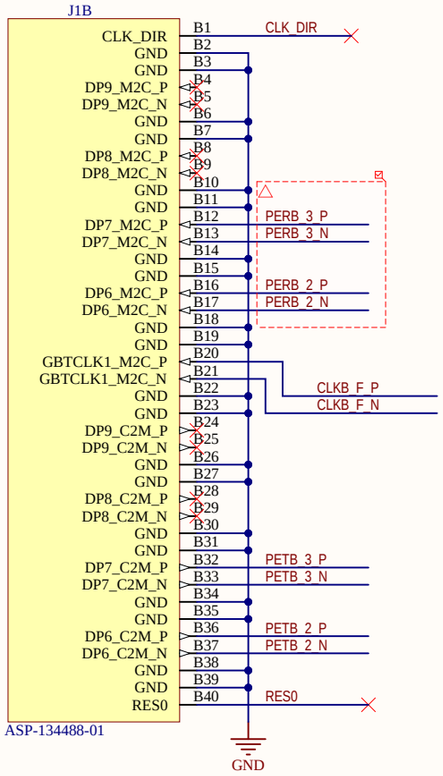
opsero ELECTRONIC DESIGN

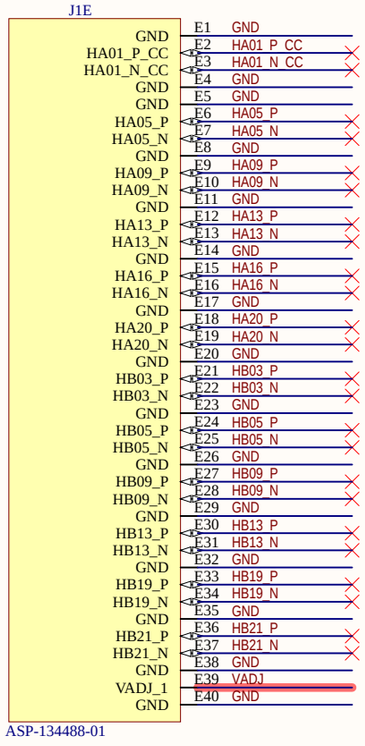
TITLE	MCIO PCIe FMC
SHEET	LPC FMC
CONFIG.	Standard
PROJECT	FPGA Drive
DRAWN	J Johnson
DATE	2026-02-03
SIZE	B
SCH P/N.	OP103-01-SCH.
REV.	A-1
SHEET OF	1 6

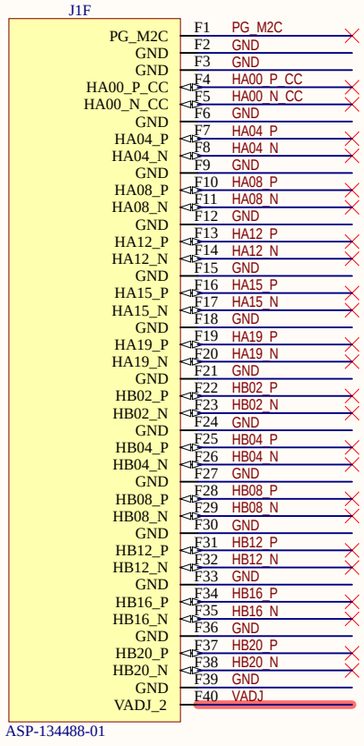
REV.	DESCRIPTION	DATE	APPROVED
A-1	First release	2026-02-03	J Johnson

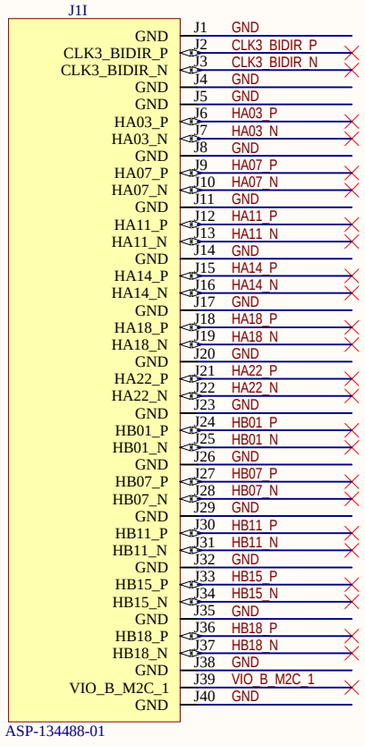
HPC FMC PINS

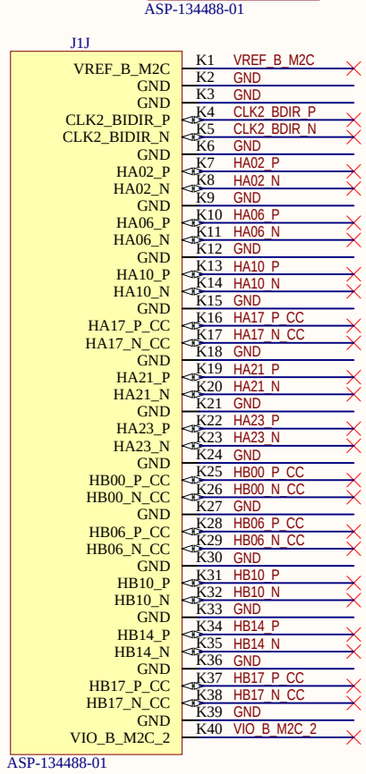












opsero ELECTRONIC DESIGN

TITLE	MCIO PCIe FMC
SHEET	HPC FMC
CONFIG.	Standard
PROJECT	FPGA Drive
DRAWN	J Johnson
DATE	2026-02-03
SIZE	B
SCH P/N.	OP103-01-SCH.
REV.	A-1
SHEET OF	2 6

REV.	DESCRIPTION	DATE	APPROVED
A-1	First release	2026-02-03	J Johnson

Routing note:
PCIe data P/N traces must be matched to 1mils

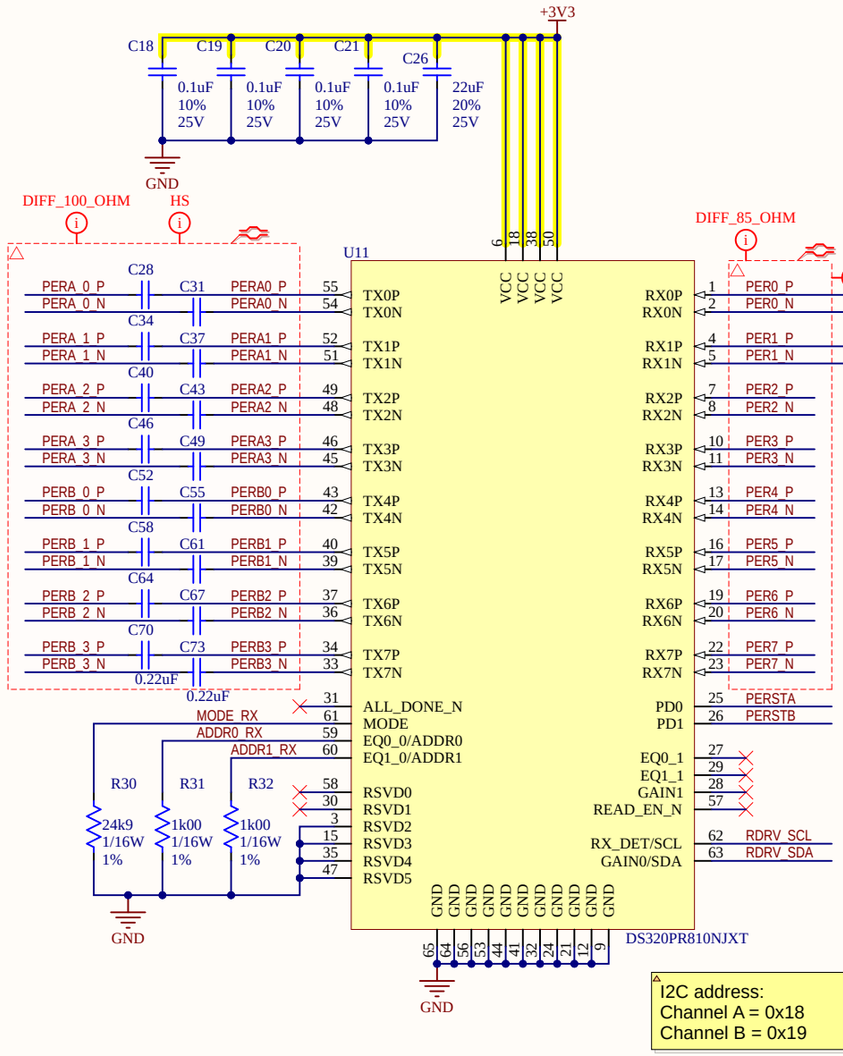
Routing note:
PCIe data pairs must be length matched to 1000mils

Routing note:
Spacing between PCIe data pairs must > 40mils

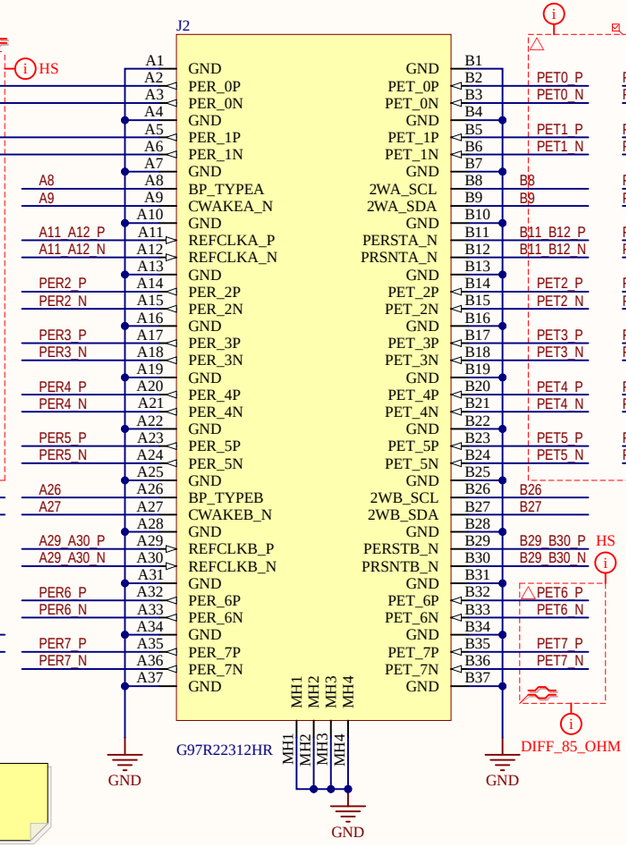
MCIO X8 SLOT
SFF-9402 HOST

J2 pin labels show the HOST configuration but the connector can be used in DEVICE mode by deasserting HOST_MODE_N.

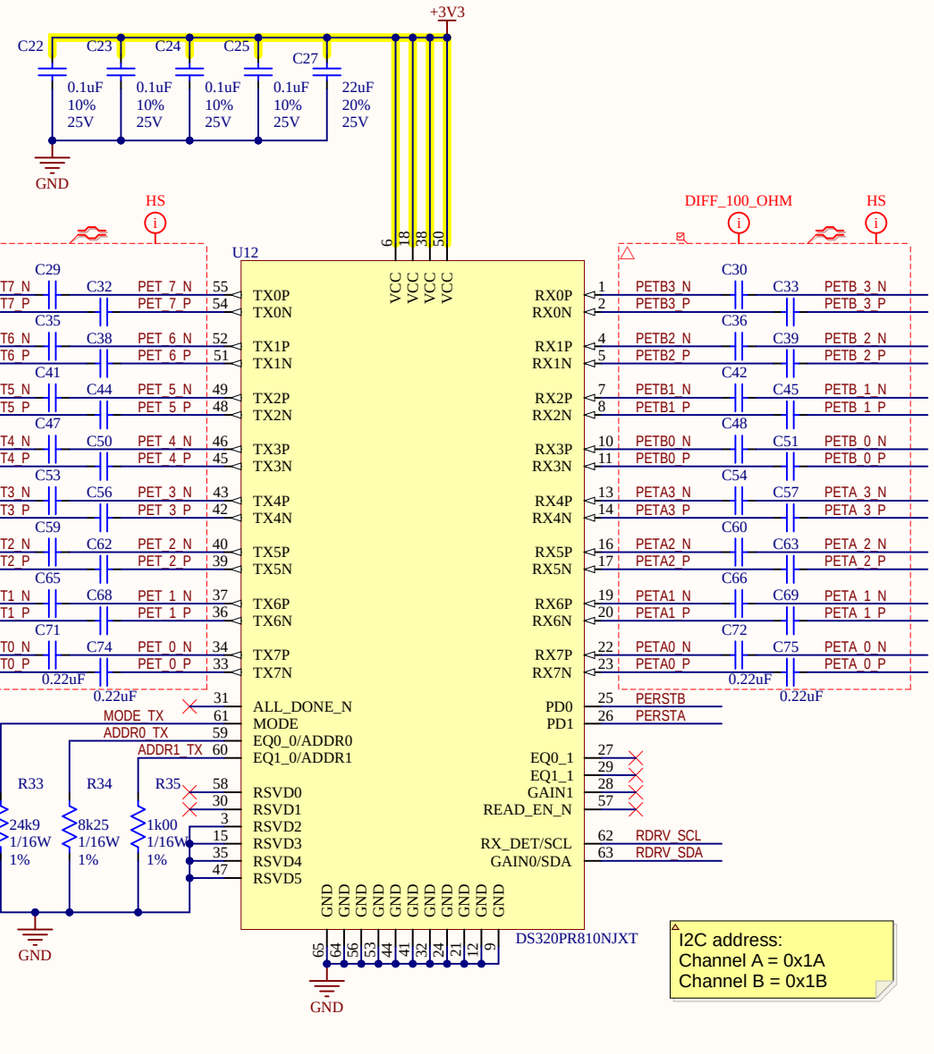
RX REDRIVER



I2C address:
Channel A = 0x18
Channel B = 0x19



TX REDRIVER



I2C address:
Channel A = 0x1A
Channel B = 0x1B

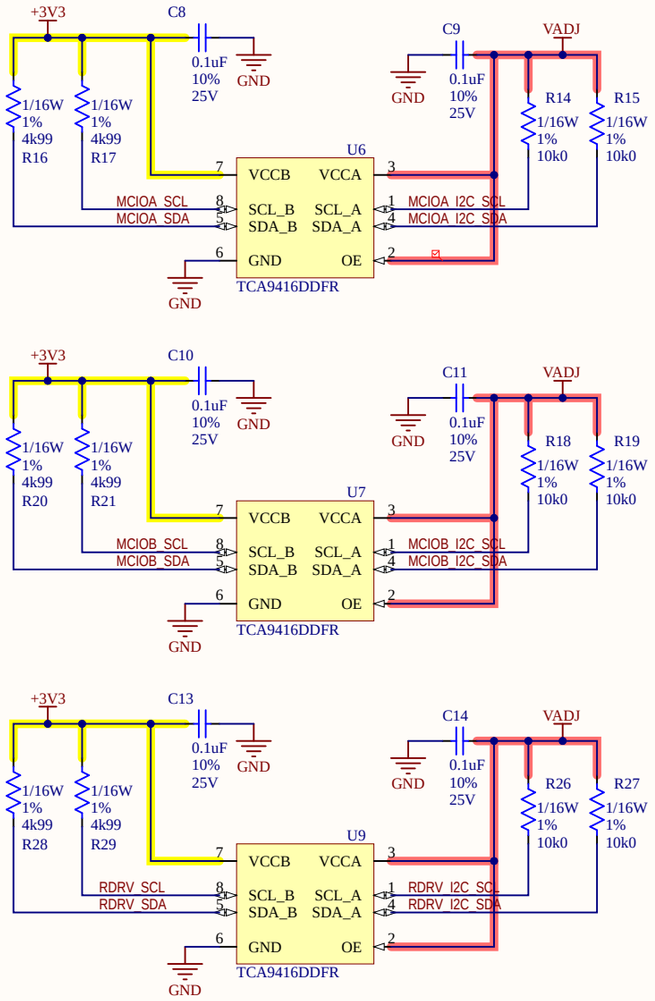
opsero ELECTRONIC DESIGN

TITLE	MCIO PCIe FMC
SHEET	MCIO Socket
CONFIG.	Standard
PROJECT	FPGA Drive
DRAWN	J Johnson
DATE	2026-02-03
SIZE	B
SCH P/N.	OP103-01-SCH.
REV.	A-1
SHEET	3 OF 6

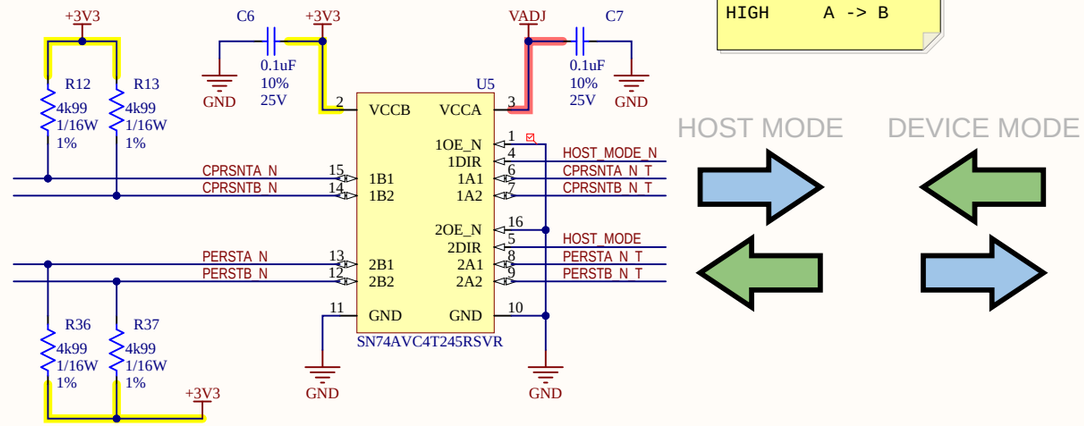
REV.	DESCRIPTION	DATE	APPROVED
A-1	First release	2026-02-03	J Johnson

PERST_N signals pulled up so that they are not floating when the MCIO cable is disconnected while in DEVICE MODE

I2C VOLTAGE TRANSLATION

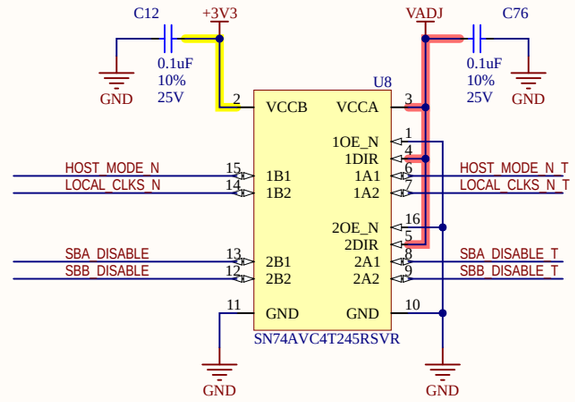


VOLTAGE TRANSLATORS



DIR INPUT	SIGNAL FLOW
LOW	B -> A
HIGH	A -> B

HOST MODE DEVICE MODE



STANDOFFS

S1

Standoff, Hex, 10mm, M2.5

S2

Standoff, Hex, 10mm, M2.5

SCREWS

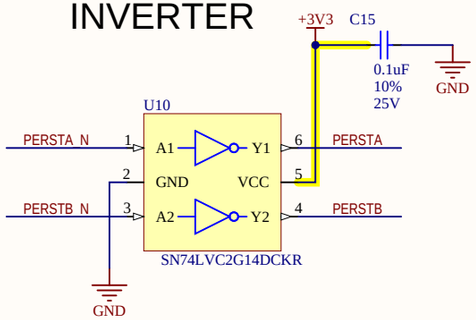
S5

Machine Screw, M2.5 thread, 4mm length

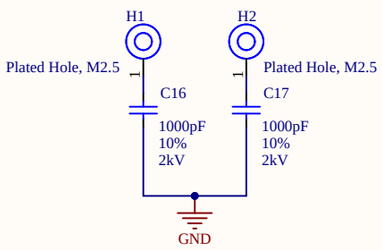
S6

Machine Screw, M2.5 thread, 4mm length

INVERTER



MOUNTING HOLES



FIDUCIALS

opsero ELECTRONIC DESIGN

TITLE	MCIO PCIe FMC
SHEET	Translators
CONFIG.	Standard
PROJECT	FPGA Drive
DRAWN	J Johnson
DATE	2026-02-03
SIZE	B
SCH P/N.	OP103-01-SCH.
REV.	A-1
SHEET OF	4 6

REV.	DESCRIPTION	DATE	APPROVED
A-1	First release	2026-02-03	J Johnson

NOTES ON SUPPORT FOR OPEN COMPUTE PROJECT M-XIO

The MCIOx8 connector on this product is wired for SFF-9402 standard by default. To make the connector compatible with OCP M-XIO standard, albeit without 3P3VAUX_MGMT, USB or FLEXIO support, assert the SBB_DISABLE input to disconnect the sideband B signals.

Alternatively one can use an MCIOx8 to 2x MCIOx4 cables to produce two MCIOx4 interfaces that are both compatible with OCP M-XIO, albeit without 3P3VAUX_MGMT or FLEXIO support.

To enable 3P3VAUX_MGMT support, jumpers R38 and R39 can be loaded with 0R resistors. However, when R38 and R39 are loaded, the HOST_MODE_N input must always be driven LOW (or left unconnected), otherwise a voltage contention will occur with MCIOA_SCL and/or MCIOB_SCL signals.

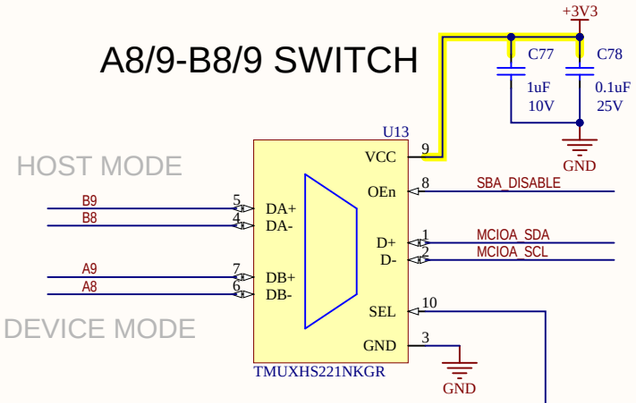
SBA_DISABLE = Disconnect sideband A signals

SBB_DISABLE = Disconnect sideband B signals

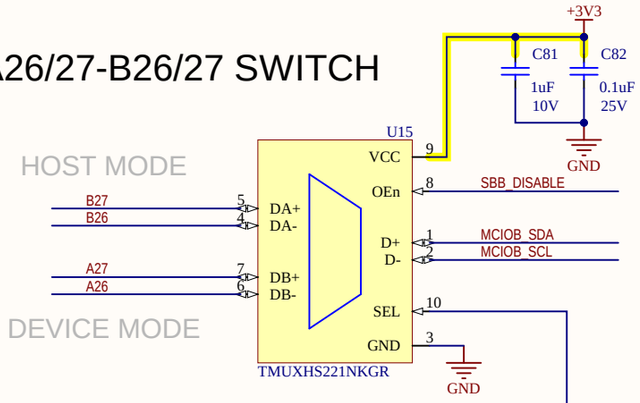
HOST_MODE_N:

LOW = HOST MODE
HIGH = DEVICE MODE

A8/9-B8/9 SWITCH

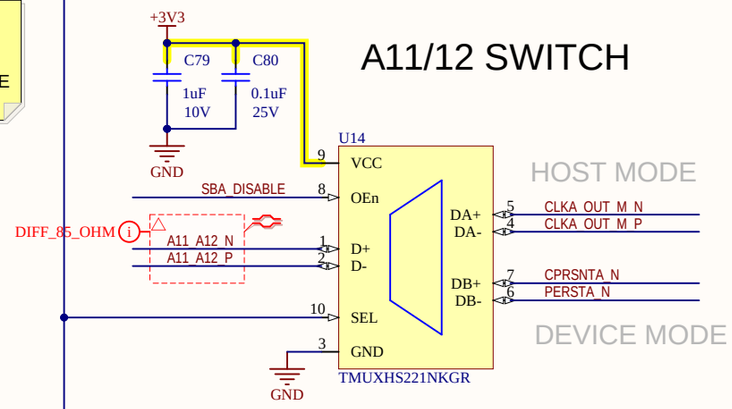


A26/27-B26/27 SWITCH

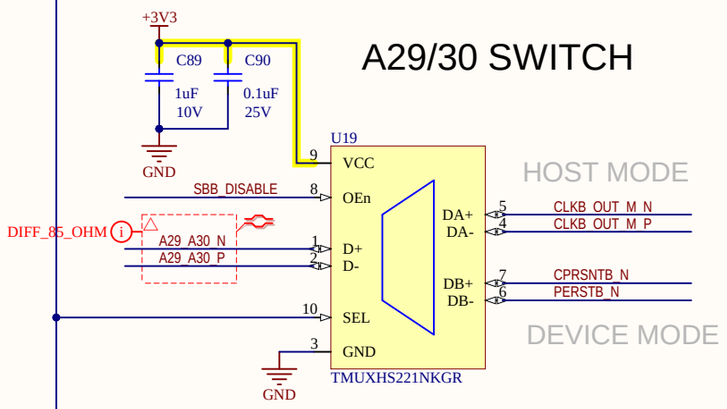


HOST_MODE_N

A11/12 SWITCH

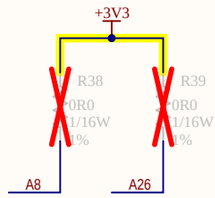


A29/30 SWITCH

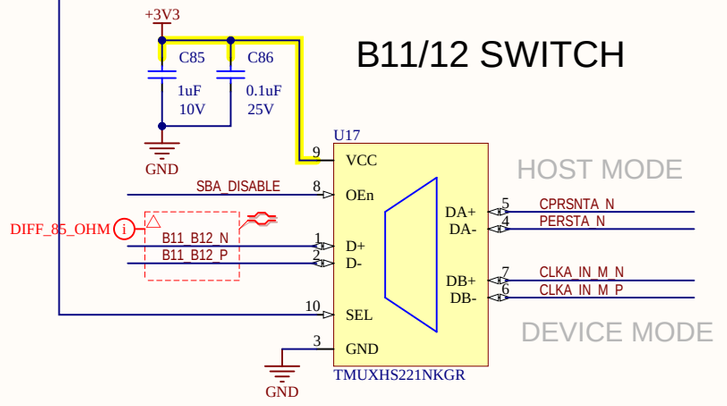


Data inputs of U13, U14, U15, U17, U19 and U20 are connected with inverted polarity to optimize PCB layout.

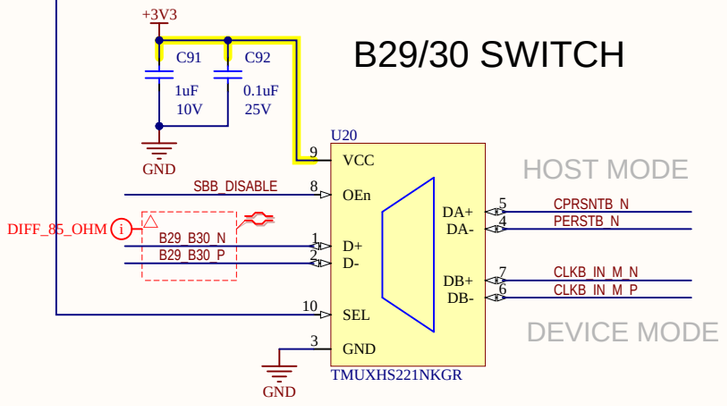
3P3VAUX_MGMT JUMPERS (NOT LOADED)



B11/12 SWITCH



B29/30 SWITCH



SEL	OEn	MUX CONFIG
LOW	LOW	D to DA
HIGH	LOW	D to DB
X	HIGH	All Hi-Z

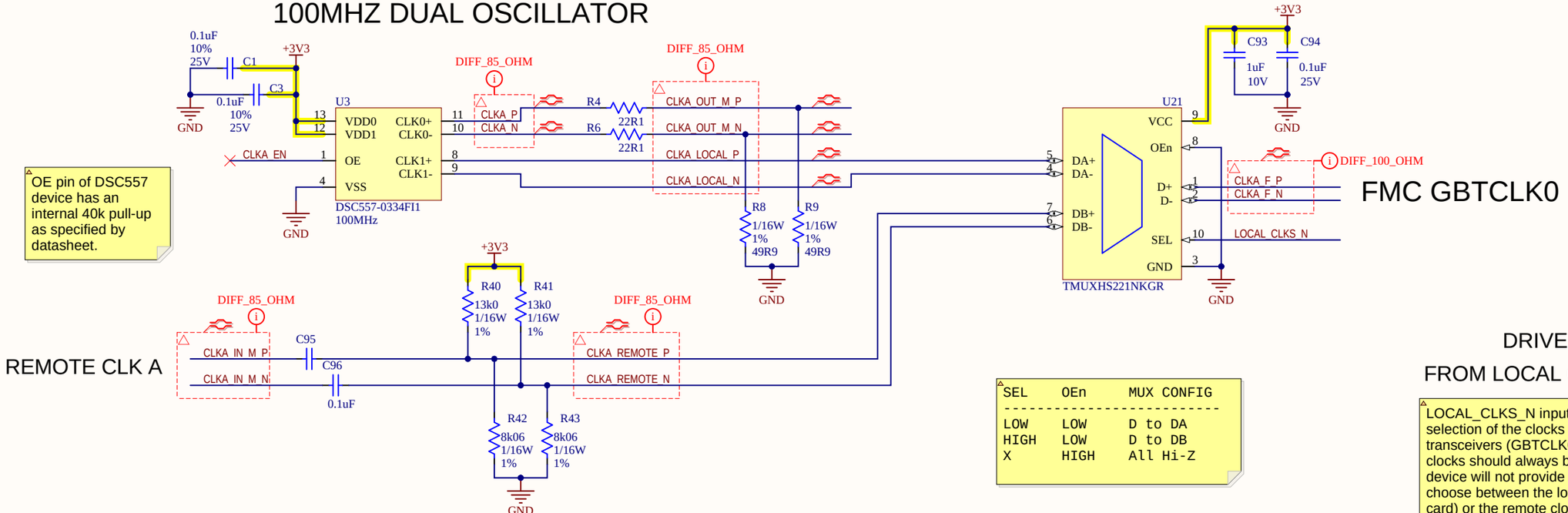
opsero ELECTRONIC DESIGN

TITLE	MCIO PCIe FMC
SHEET	Switches
CONFIG.	Standard
PROJECT	FPGA Drive
DRAWN	J Johnson
DATE	2026-02-03
SIZE	B
SCH P/N.	OP103-01-SCH.
REV.	A-1
SHEET OF	5 6

REV.	DESCRIPTION	DATE	APPROVED
A-1	First release	2026-02-03	J Johnson

CLKA/B_F_P/N PCIe reference clock connects to GBTCLK of the FMC, thus it is required to be LVDS according to Rule 5.54: The reference clocks, GBTCLK, shall use the LVDS signaling standard

100MHZ DUAL OSCILLATOR

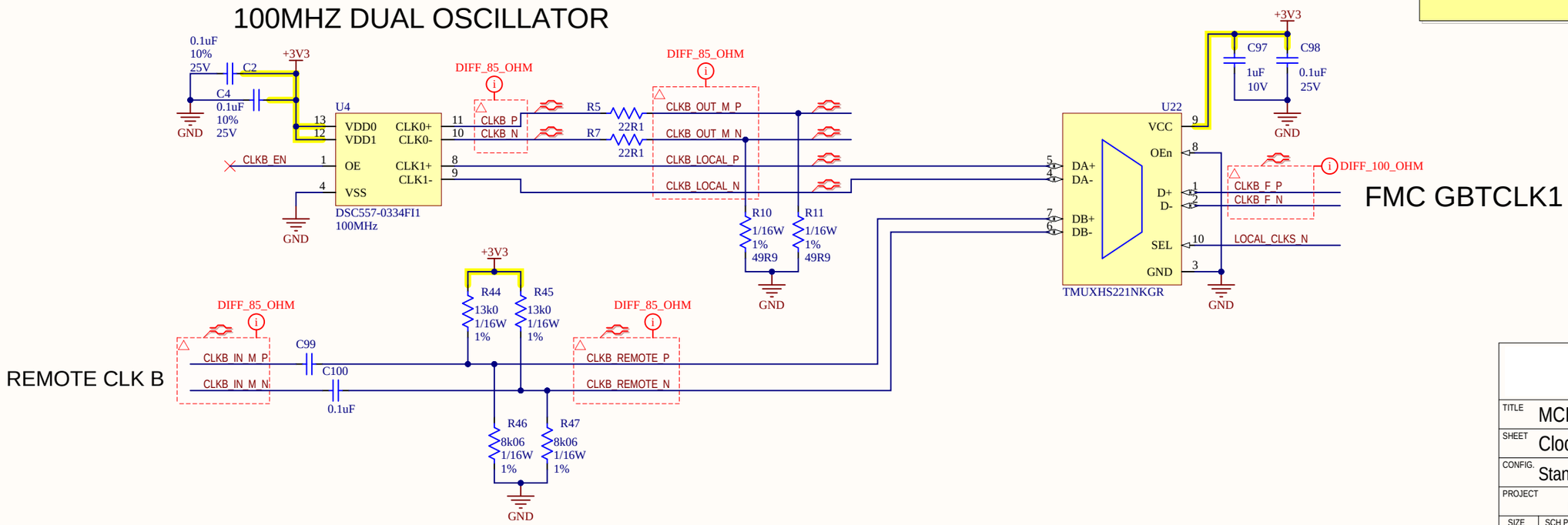


SEL	OEn	MUX CONFIG
LOW	LOW	D to DA
HIGH	LOW	D to DB
X	HIGH	All Hi-Z

DRIVE FMC GBTCLK0/1 FROM LOCAL OR REMOTE CLOCKS

LOCAL_CLKS_N input to the MCIO PCIe FMC allows selection of the clocks that are used to drive the gigabit transceivers (GBTCLK0/1). In HOST MODE, the local clocks should always be used since the connected MCIO device will not provide a clock. In DEVICE MODE, we can choose between the local clocks (generated by the FMC card) or the remote clocks provided by the MCIO host.

100MHZ DUAL OSCILLATOR



opsero ELECTRONIC DESIGN

TITLE	MCIO PCIe FMC
SHEET	Clocks
CONFIG.	Standard
PROJECT	FPGA Drive
DRAWN	J Johnson
DATE	2026-02-03
SIZE	B
SCH P/N.	OP103-01-SCH.
REV.	A-1
SHEET OF	6 6