REV.	DESCRIPTION	DATE	APPROVED
A-2	LEDs changed to standard intensity Buck converter input caps to 22uF 25V	2024-04-19	J Johnson

STANDOFFS

S1

Standoff, Hex, 10mm, M2.5

S2

Standoff, Hex, 10mm, M2.5

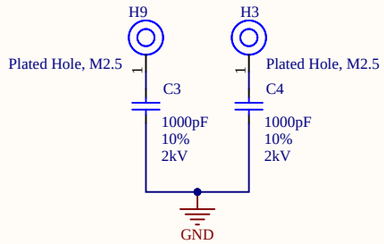
S3

Standoff, Hex, 10mm, M2.5

S4

Standoff, Hex, 10mm, M2.5

MOUNTING HOLES



FIDUCIALS

SCREWS

S5

Machine Screw, M2.5 thread, 4mm length

S6

Machine Screw, M2.5 thread, 4mm length

S7

Machine Screw, M2.5 thread, 4mm length

S11

Machine Screw, M2.5 thread, 4mm length

M.2 MODULE FIXING PARTS

SO1

Standoff, Round, Nylon, 1.6mm

S9

Machine Screw, M2.5 thread, 3mm length
388-238

SO2

Standoff, Round, Nylon, 1.6mm

S8

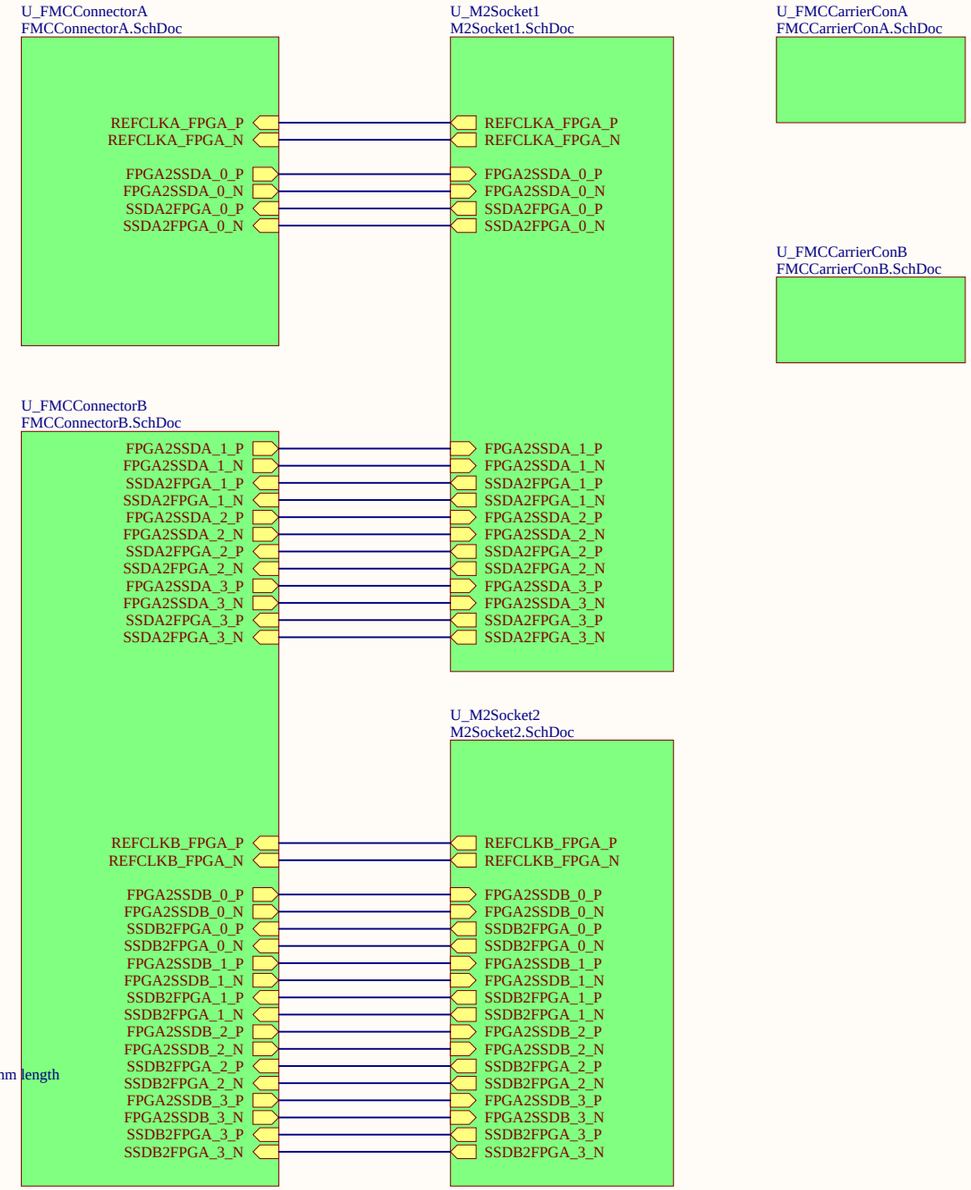
Machine Screw, M2.5 thread, 3mm length
388-238

SO6

Standoff, Round, 2.5mm, M2.5

SO3

Standoff, Round, 2.5mm, M2.5



opsero ELECTRONIC DESIGN

TITLE	M.2 M-key Stack FMC		
SHEET	Top		
CONFIG.	Standard		
PROJECT	FPGA Drive	DRAWN J Johnson	DATE 2024-01-24
SIZE B	SCH P/N. OP073-01-SCH.	REV. A-2	SHEET 1 OF 7

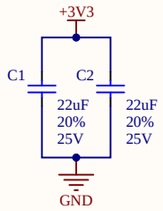
REV.	DESCRIPTION	DATE	APPROVED
A-2	LEDs changed to standard intensity Buck converter input caps to 22uF 25V	2024-04-19	J Johnson

Routing note:
PCIe data P/N traces must be matched to 5mils

Routing note:
PCIe data pairs must be length matched to 1000mils

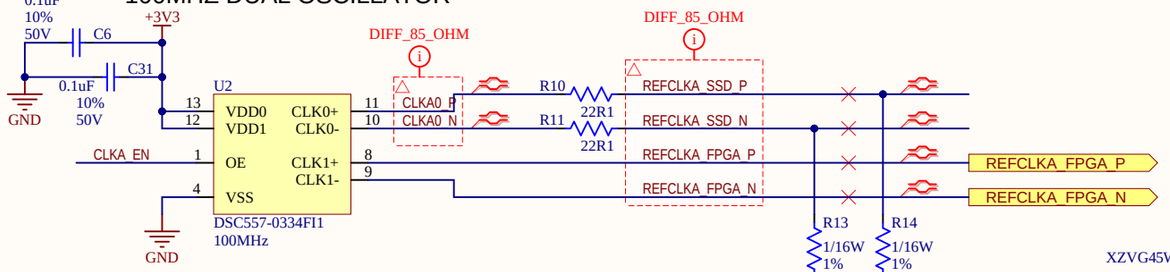
Routing note:
Spacing between PCIe data pairs must > 40mils

DECOUPLING CAPS



OE pin of DSC557 device has an internal 40k pull-up as specified by datasheet.

100MHZ DUAL OSCILLATOR



REFCLK_FPGA_P/N PCIe reference clock connects to GBTCLK of the FMC, thus it is required to be LVDS according to Rule 5.54: The reference clocks, GBTCLK, shall use the LVDS signaling standard

Sleep mode clock feature not supported.
SUSCLK (32kHz clock input) is not connected at the host.

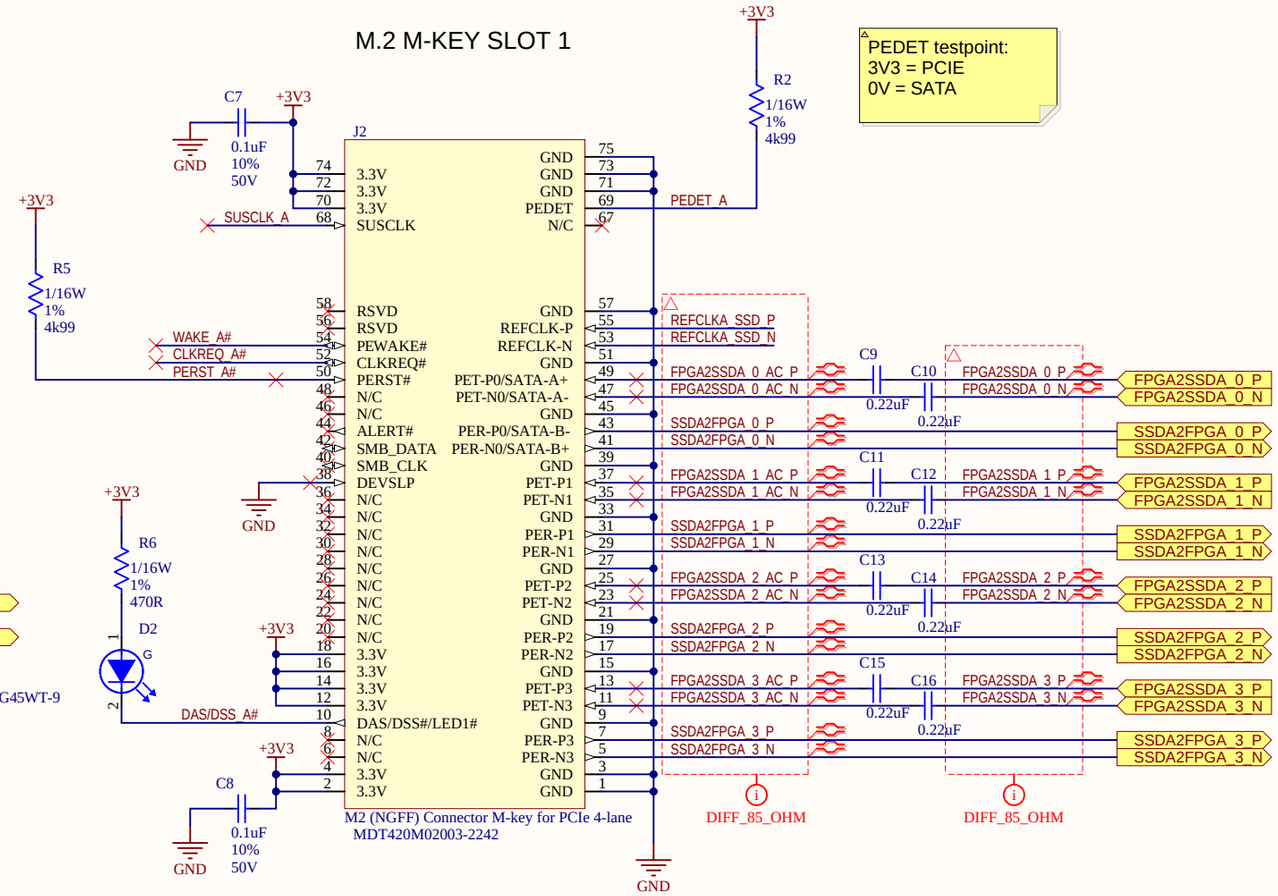
Reference clock parking not supported.
CLKREQ# (open drain output driven by M2 module) is not connected at the host.

WAKE feature not supported.
WAKE# (open drain output driven by M2 module) is not connected at the host.

DEVSLP Sleep mode not supported.
DEVSLP input is tied to ground at the host.

M.2 Slot 1 is powered by the FMC connector's 12V supply which is converted to 3.3V by DC-DC converter TPS565247DRLR (see sheet 3).

M.2 M-KEY SLOT 1



XZVG45WT-9

TITLE	M.2 M-key Stack FMC		
SHEET	M.2 Socket 1		
CONFIG.	Standard		
PROJECT	FPGA Drive	DRAWN J Johnson	DATE 2024-01-24
SIZE B	SCH P/N. OP073-01-SCH.	REV. A-2	SHEET 2 OF 7

REV.	DESCRIPTION	DATE	APPROVED
A-2	LEDs changed to standard intensity Buck converter input caps to 22uF 25V	2024-04-19	J Johnson

Routing note:
PCIe data P/N traces must be matched to 5mils

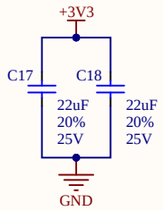
Routing note:
PCIe data pairs must be length matched to 1000mils

Routing note:
Spacing between PCIe data pairs must > 40mils

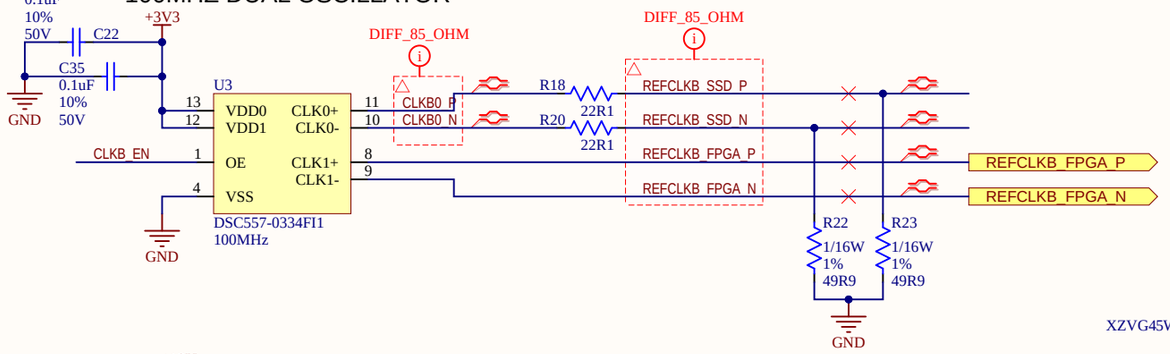
OE pin of DSC557 device has an internal 40k pull-up as specified by datasheet.

REFCLK_FPGA_P/N PCIe reference clock connects to GBTCLK of the FMC, thus it is required to be LVDS according to Rule 5.54: The reference clocks, GBTCLK, shall use the LVDS signaling standard

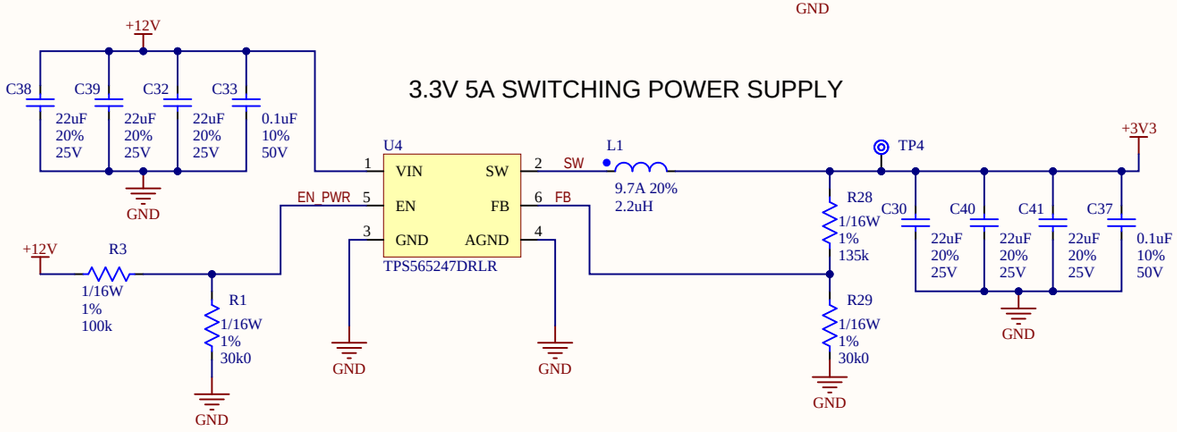
DECOUPLING CAPS



100MHZ DUAL OSCILLATOR



3.3V 5A SWITCHING POWER SUPPLY



Sleep mode clock feature not supported.
SUSCLK (32kHz clock input) is not connected at the host.

Reference clock parking not supported.
CLKREQ# (open drain output driven by M2 module) is not connected at the host.

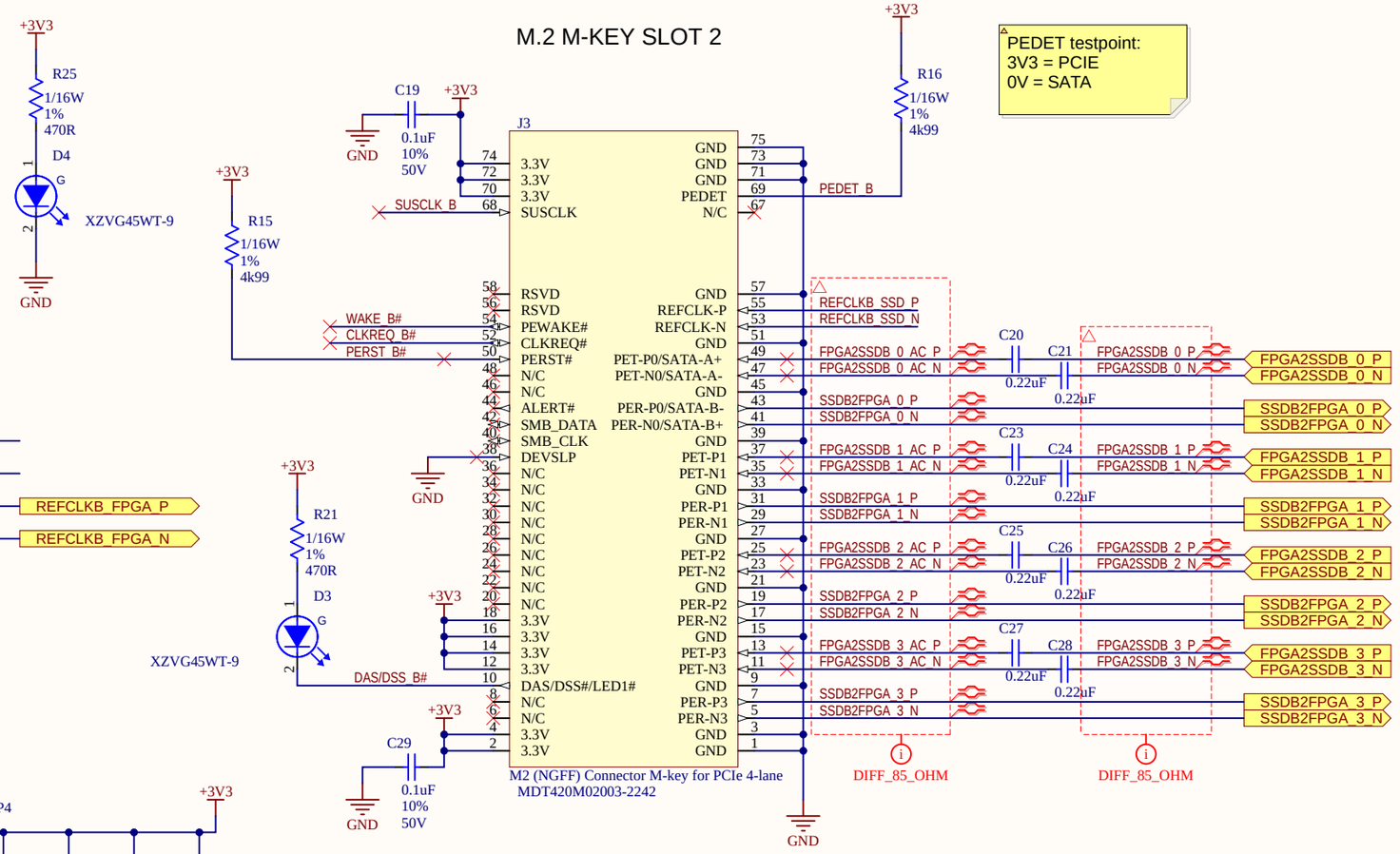
WAKE feature not supported.
WAKE# (open drain output driven by M2 module) is not connected at the host.

DEVSLP Sleep mode not supported.
DEVSLP input is tied to ground at the host.

M.2 Slot 2 is powered by the FMC connector's 12V supply which is converted to 3.3V by DC-DC converter TPS565247DRLR (see below).

PEDET testpoint:
3V3 = PCIE
0V = SATA

M.2 M-KEY SLOT 2



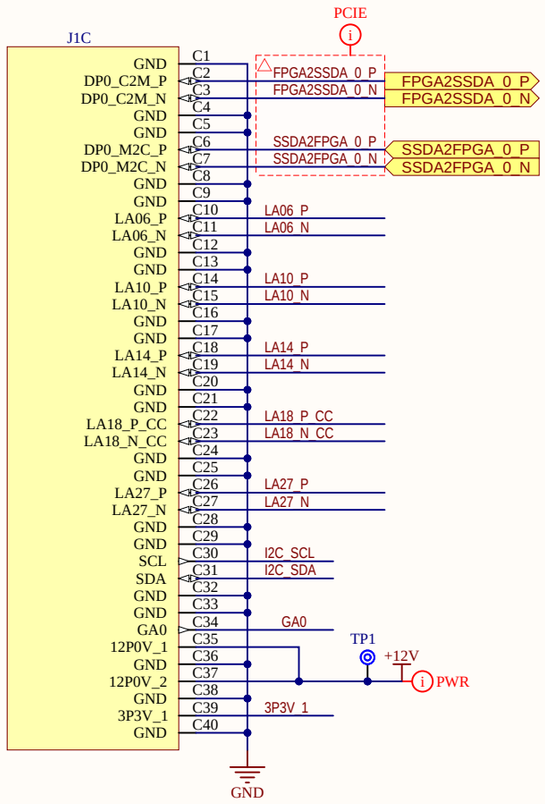
According to M.2 standard, M.2 M-key modules are rated for 2.5A max continuous. Efficiency of the DC-DC converter TPS565247DRLR is > 90% at an output current of 5A (assuming 2x M.2 modules operating at the maximum rated load of 8.25W each) which equates to a current draw on the 12V rail of less than 1.53A. The VITA 57.1 standard specifies a minimum capacity of only 1A on the 12V rail. For this reason, if you intend to use 2x M.2 modules at full rated load (8.25W each), it is necessary to confirm that the carrier board is capable of supplying sufficient current on the 12V rail.

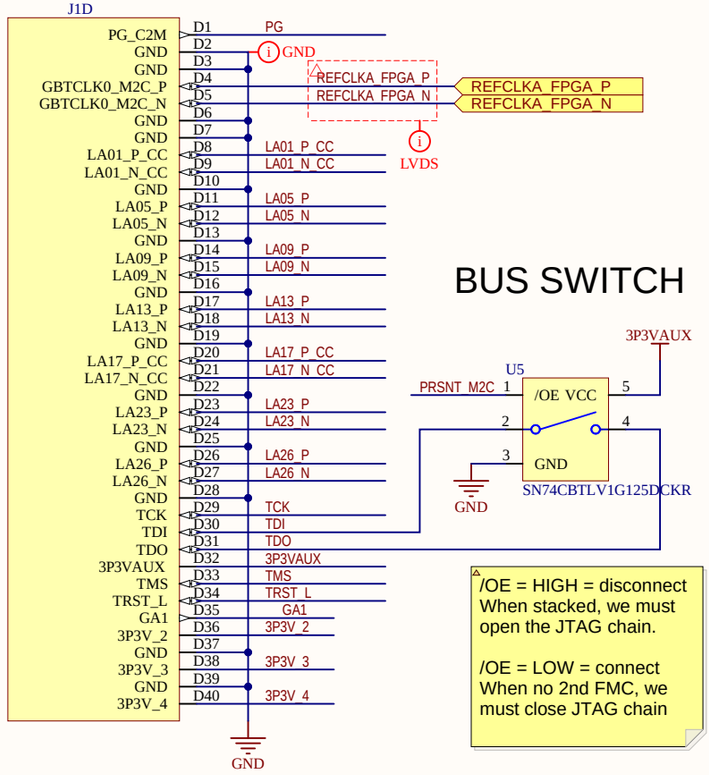
opsero ELECTRONIC DESIGN

TITLE	M.2 M-key Stack FMC
SHEET	M.2 Socket 2
CONFIG.	Standard
PROJECT	FPGA Drive
DRAWN	J Johnson
DATE	2024-01-24
SIZE	B
SCH P/N.	OP073-01-SCH.
REV.	A-2
SHEET	3 OF 7

REV.	DESCRIPTION	DATE	APPROVED
A-2	LEDs changed to standard intensity Buck converter input caps to 22uF 25V	2024-04-19	J Johnson

FMC PINS COMMON WITH LPC

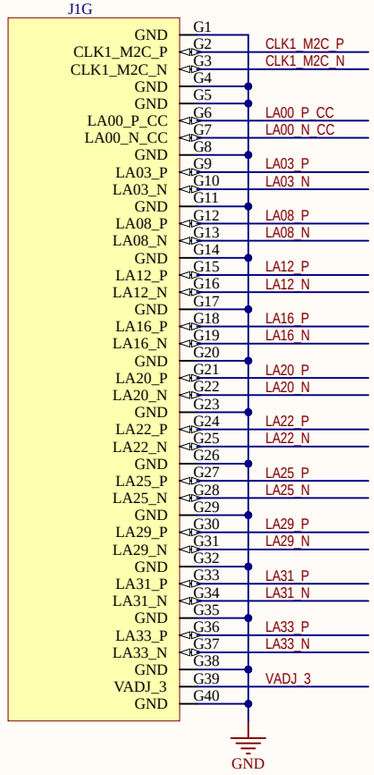


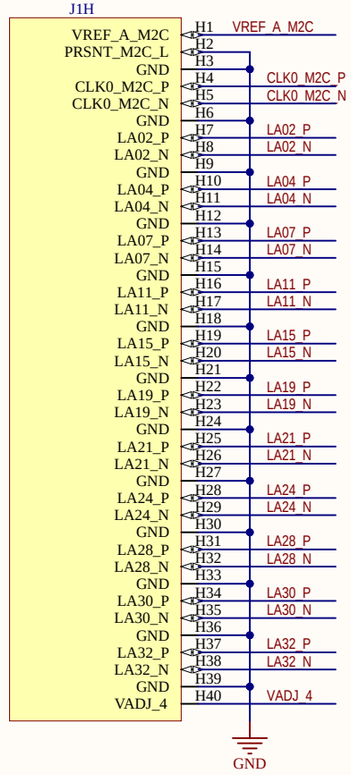


BUS SWITCH

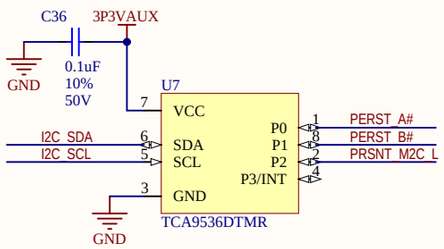
/OE = HIGH = disconnect
When stacked, we must open the JTAG chain.

/OE = LOW = connect
When no 2nd FMC, we must close JTAG chain



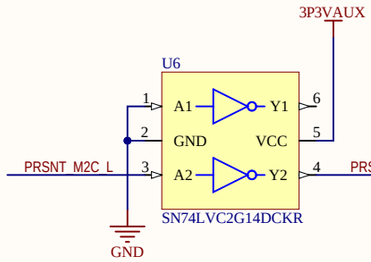


I2C I/O EXTENDER



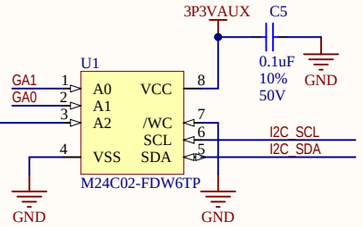
I/O ports default to input state on power-up

INVERTER



In accordance with the VITA 57.1 standard:
GA0 goes to A1, GA1 goes to A0

EEPROM



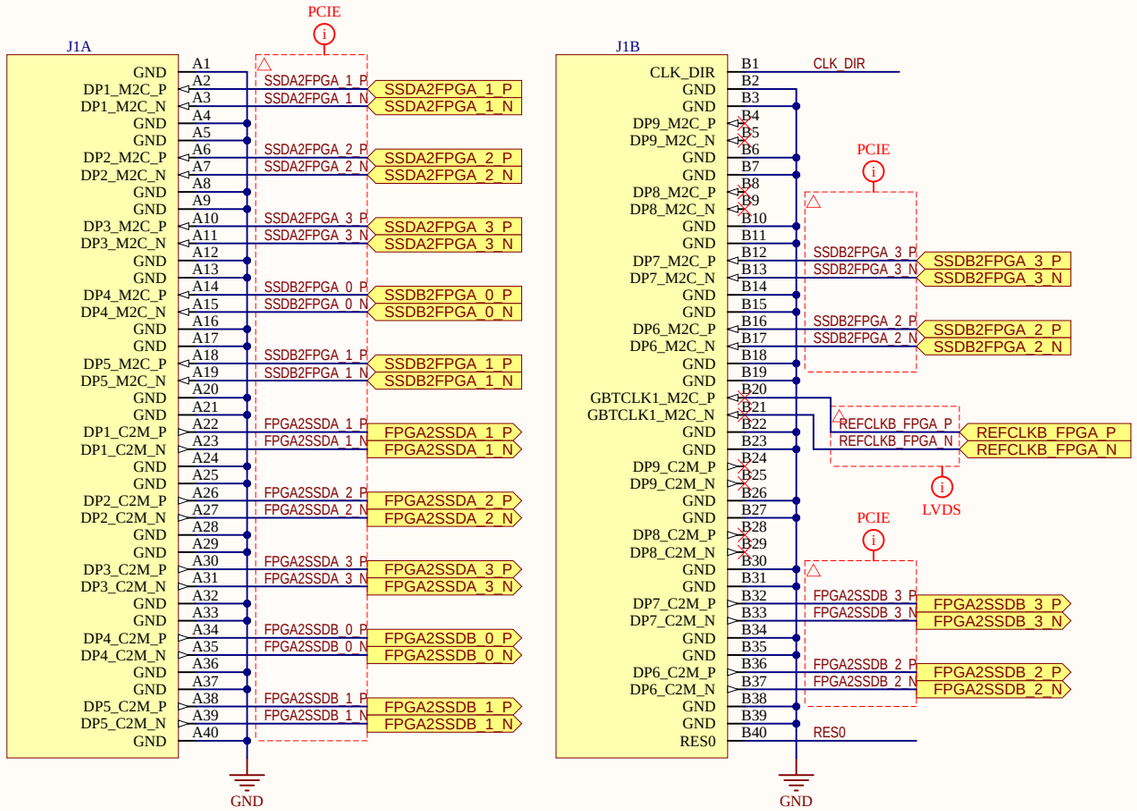
When the 2nd FMC is loaded, we change EEPROM address so that the 2nd FMC determines VADJ

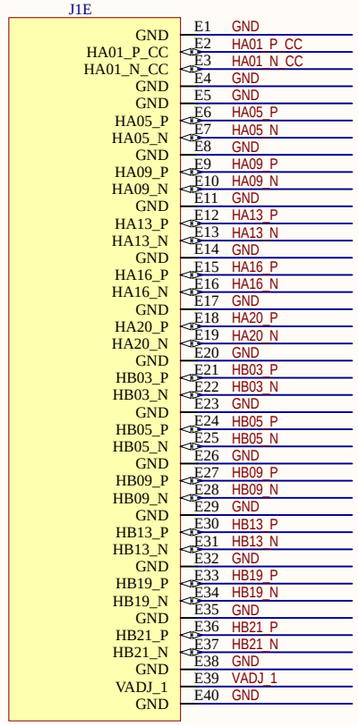
opsero ELECTRONIC DESIGN

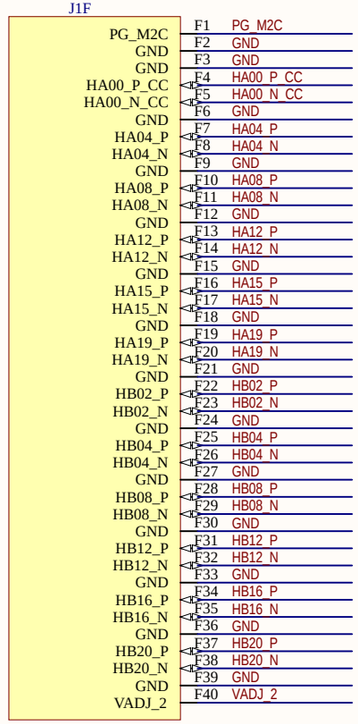
TITLE	M.2 M-key Stack FMC		
SHEET	LPC FMC		
CONFIG.	Standard		
PROJECT	FPGA Drive	DRAWN J Johnson	DATE 2024-01-24
SIZE B	SCH P/N. OP073-01-SCH.	REV. A-2	SHEET 4 OF 7

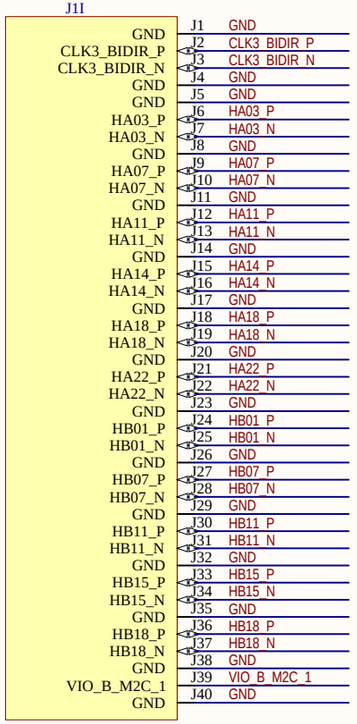
REV.	DESCRIPTION	DATE	APPROVED
A-2	LEDs changed to standard intensity Buck converter input caps to 22uF 25V	2024-04-19	J Johnson

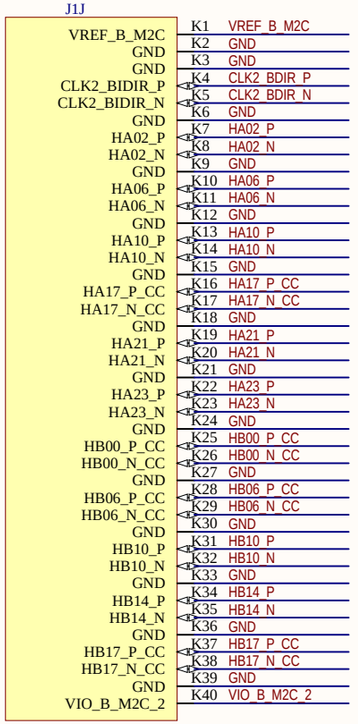
HPC FMC PINS











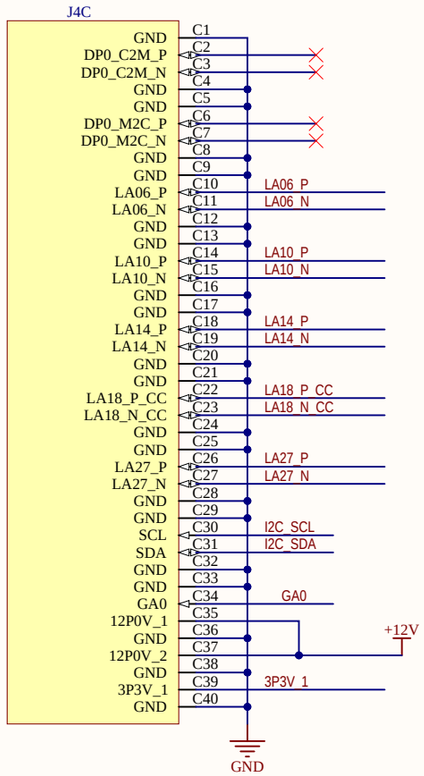
opsero ELECTRONIC DESIGN

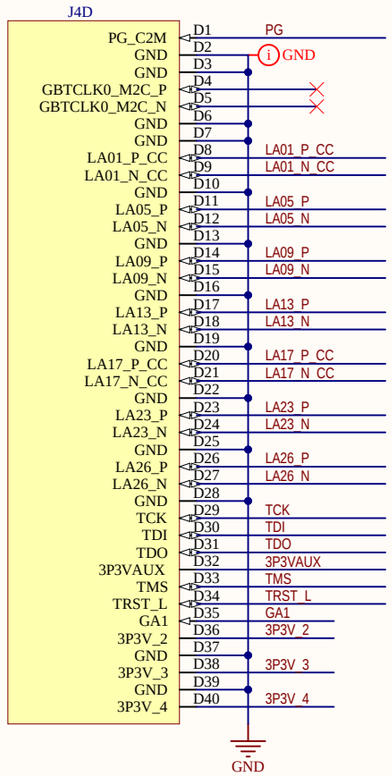
TITLE	M.2 M-key Stack FMC		
SHEET	HPC FMC		
CONFIG.	Standard		
PROJECT	FPGA Drive	DRAWN J Johnson	DATE 2024-01-24
SIZE B	SCH P/N. OP073-01-SCH.	REV. A-2	SHEET 5 OF 7

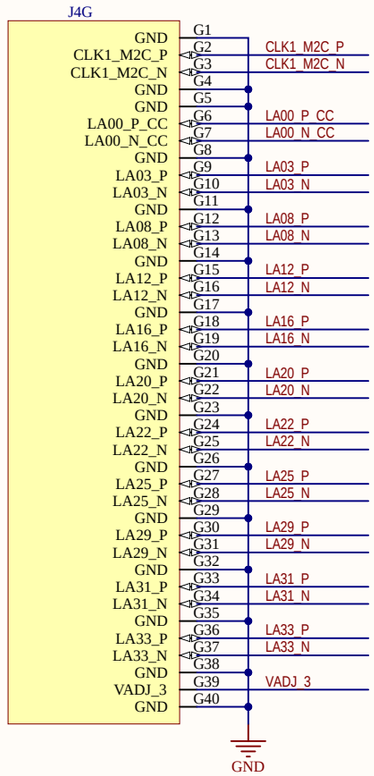
REV.	DESCRIPTION	DATE	APPROVED
A-2	LEDs changed to standard intensity Buck converter input caps to 22uF 25V	2024-04-19	J Johnson

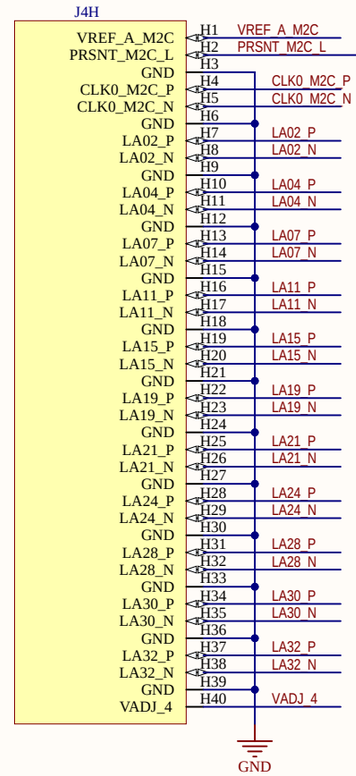
FMC PINS COMMON WITH LPC

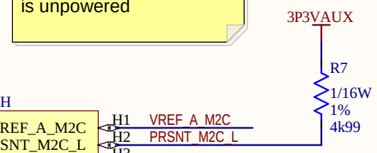
Pull-up to 3.3VAUX so that we are able change EEPROM address if required, even when FMC is unpowered











TITLE	M.2 M-key Stack FMC
SHEET	Carrier LPC FMC
CONFIG.	Standard
PROJECT	FPGA Drive
DRAWN	J Johnson
DATE	2024-01-24
SIZE	B
SCH P/N.	OP073-01-SCH.
REV.	A-2
SHEET OF	6 7

REV.	DESCRIPTION	DATE	APPROVED
A-2	LEDs changed to standard intensity Buck converter input caps to 22uF 25V	2024-04-19	J Johnson

HPC FMC PINS

J4A

GND	A1	
DP1_M2C_P	A2	
DP1_M2C_N	A3	
GND	A4	
GND	A5	
DP2_M2C_P	A6	
DP2_M2C_N	A7	
GND	A8	
GND	A9	
DP3_M2C_P	A10	
DP3_M2C_N	A11	
GND	A12	
GND	A13	
DP4_M2C_P	A14	
DP4_M2C_N	A15	
GND	A16	
GND	A17	
DP5_M2C_P	A18	
DP5_M2C_N	A19	
GND	A20	
GND	A21	
DP1_C2M_P	A22	
DP1_C2M_N	A23	
GND	A24	
GND	A25	
DP2_C2M_P	A26	
DP2_C2M_N	A27	
GND	A28	
GND	A29	
DP3_C2M_P	A30	
DP3_C2M_N	A31	
GND	A32	
GND	A33	
DP4_C2M_P	A34	
DP4_C2M_N	A35	
GND	A36	
GND	A37	
DP5_C2M_P	A38	
DP5_C2M_N	A39	
GND	A40	

GND

J4B

CLK_DIR	B1	CLK_DIR
GND	B2	
GND	B3	
DP9_M2C_P	B4	
DP9_M2C_N	B5	
GND	B6	
GND	B7	
DP8_M2C_P	B8	
DP8_M2C_N	B9	
GND	B10	
GND	B11	
DP7_M2C_P	B12	
DP7_M2C_N	B13	
GND	B14	
GND	B15	
DP6_M2C_P	B16	
DP6_M2C_N	B17	
GND	B18	
GND	B19	
GBTCLK1_M2C_P	B20	
GBTCLK1_M2C_N	B21	
GND	B22	
GND	B23	
DP9_C2M_P	B24	
DP9_C2M_N	B25	
GND	B26	
GND	B27	
DP8_C2M_P	B28	
DP8_C2M_N	B29	
GND	B30	
GND	B31	
DP7_C2M_P	B32	
DP7_C2M_N	B33	
GND	B34	
GND	B35	
DP6_C2M_P	B36	
DP6_C2M_N	B37	
GND	B38	
GND	B39	
RES0	B40	RES0

GND

J4E

GND	E1	GND
HA01_P_CC	E2	HA01_P_CC
HA01_N_CC	E3	HA01_N_CC
GND	E4	GND
GND	E5	GND
HA05_P	E6	HA05_P
HA05_N	E7	HA05_N
GND	E8	GND
HA09_P	E9	HA09_P
HA09_N	E10	HA09_N
GND	E11	GND
HA13_P	E12	HA13_P
HA13_N	E13	HA13_N
GND	E14	GND
HA16_P	E15	HA16_P
HA16_N	E16	HA16_N
GND	E17	GND
HA20_P	E18	HA20_P
HA20_N	E19	HA20_N
GND	E20	GND
HB03_P	E21	HB03_P
HB03_N	E22	HB03_N
GND	E23	GND
HB05_P	E24	HB05_P
HB05_N	E25	HB05_N
GND	E26	GND
HB09_P	E27	HB09_P
HB09_N	E28	HB09_N
GND	E29	GND
HB13_P	E30	HB13_P
HB13_N	E31	HB13_N
GND	E32	GND
HB19_P	E33	HB19_P
HB19_N	E34	HB19_N
GND	E35	GND
HB21_P	E36	HB21_P
HB21_N	E37	HB21_N
GND	E38	GND
VADJ_1	E39	VADJ_1
GND	E40	GND

J4F

PG_M2C	F1	PG_M2C
GND	F2	GND
GND	F3	GND
HA00_P_CC	F4	HA00_P_CC
HA00_N_CC	F5	HA00_N_CC
GND	F6	GND
HA04_P	F7	HA04_P
HA04_N	F8	HA04_N
GND	F9	GND
HA08_P	F10	HA08_P
HA08_N	F11	HA08_N
GND	F12	GND
HA12_P	F13	HA12_P
HA12_N	F14	HA12_N
GND	F15	GND
HA15_P	F16	HA15_P
HA15_N	F17	HA15_N
GND	F18	GND
HA19_P	F19	HA19_P
HA19_N	F20	HA19_N
GND	F21	GND
HB02_P	F22	HB02_P
HB02_N	F23	HB02_N
GND	F24	GND
HB04_P	F25	HB04_P
HB04_N	F26	HB04_N
GND	F27	GND
HB08_P	F28	HB08_P
HB08_N	F29	HB08_N
GND	F30	GND
HB12_P	F31	HB12_P
HB12_N	F32	HB12_N
GND	F33	GND
HB16_P	F34	HB16_P
HB16_N	F35	HB16_N
GND	F36	GND
HB20_P	F37	HB20_P
HB20_N	F38	HB20_N
GND	F39	GND
VADJ_2	F40	VADJ_2

J4I

GND	J1	GND
CLK3_BIDIR_P	J2	CLK3_BIDIR_P
CLK3_BIDIR_N	J3	CLK3_BIDIR_N
GND	J4	GND
GND	J5	GND
HA03_P	J6	HA03_P
HA03_N	J7	HA03_N
GND	J8	GND
HA07_P	J9	HA07_P
HA07_N	J10	HA07_N
GND	J11	GND
HA11_P	J12	HA11_P
HA11_N	J13	HA11_N
GND	J14	GND
HA14_P	J15	HA14_P
HA14_N	J16	HA14_N
GND	J17	GND
HA18_P	J18	HA18_P
HA18_N	J19	HA18_N
GND	J20	GND
HA22_P	J21	HA22_P
HA22_N	J22	HA22_N
GND	J23	GND
HB01_P	J24	HB01_P
HB01_N	J25	HB01_N
GND	J26	GND
HB07_P	J27	HB07_P
HB07_N	J28	HB07_N
GND	J29	GND
HB11_P	J30	HB11_P
HB11_N	J31	HB11_N
GND	J32	GND
HB15_P	J33	HB15_P
HB15_N	J34	HB15_N
GND	J35	GND
HB18_P	J36	HB18_P
HB18_N	J37	HB18_N
GND	J38	GND
VIO_B_M2C_1	J39	VIO_B_M2C_1
GND	J40	GND

J4J

VREF_B_M2C	K1	VREF_B_M2C
GND	K2	GND
GND	K3	GND
CLK2_BIDIR_P	K4	CLK2_BDIR_P
CLK2_BIDIR_N	K5	CLK2_BDIR_N
GND	K6	GND
HA02_P	K7	HA02_P
HA02_N	K8	HA02_N
GND	K9	GND
HA06_P	K10	HA06_P
HA06_N	K11	HA06_N
GND	K12	GND
HA10_P	K13	HA10_P
HA10_N	K14	HA10_N
GND	K15	GND
HA17_P_CC	K16	HA17_P_CC
HA17_N_CC	K17	HA17_N_CC
GND	K18	GND
HA21_P	K19	HA21_P
HA21_N	K20	HA21_N
GND	K21	GND
HA23_P	K22	HA23_P
HA23_N	K23	HA23_N
GND	K24	GND
HB00_P_CC	K25	HB00_P_CC
HB00_N_CC	K26	HB00_N_CC
GND	K27	GND
HB06_P_CC	K28	HB06_P_CC
HB06_N_CC	K29	HB06_N_CC
GND	K30	GND
HB10_P	K31	HB10_P
HB10_N	K32	HB10_N
GND	K33	GND
HB14_P	K34	HB14_P
HB14_N	K35	HB14_N
GND	K36	GND
HB17_P_CC	K37	HB17_P_CC
HB17_N_CC	K38	HB17_N_CC
GND	K39	GND
VIO_B_M2C_2	K40	VIO_B_M2C_2

opsero ELECTRONIC DESIGN

TITLE: M.2 M-key Stack FMC			
SHEET: Carrier HPC FMC			
CONFIG.: Standard			
PROJECT: FPGA Drive	DRAWN: J Johnson	DATE: 2024-01-24	
SIZE: B	SCH P/N.: OP073-01-SCH.	REV.: A-2	SHEET 7 OF 7