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PCIe Gen5 Signal Integrity Implementation - Issues & Solutions

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Abstract

In a rare move PCIe Gen5 leap-frogged industry data rates, pushing mainstream implementation to 32 Gbps. While Gen4 struggled with discontinuities as the primary cause of link failure, Gen5 swings the pendulum back to the necessity of handling both discontinuities and loss. This paper presents SI lessons learned during the implementation of large systems with hundreds of Gen5 signals, explaining how addressing loss and discontinuities relates to PCBs, cables, equalization, simulation/measurement, retimers, and manufacturing issues for both host and add-in card design implementation. As all serial links are similar at the electrical level, the issues and solutions described are applicable to all types of serial link design above 30 Gbps.

Author's Biographies

Donald Telian. Signal Integrity Consultant, SiGuys, and author of "Signal Integrity, In Practice". Building on 40 years of SI experience at Intel, Cadence, HP, and others, his focus is helping customers implement today's highest-speed serial links. With tens of thousands of serial links in production spanning all types of electronic standards and products, he consistently helps customers migrate to next-generation data rates again and again. Donald is widely known as the SI designer of the PCI bus and the originator of IBIS modeling and has taught SI techniques to thousands of engineers in more than 15 countries. His new book "Signal Integrity, In Practice" brings fresh articulation to the changing practice of SI in the decades ahead. This book and his numerous published works are available at siguys.com.

Kevin Rowett. VP, Systems Engineering, Xconn Technologies – Owner, Iron Heart Consulting. Providing engineering consulting services for technology companies at all stages and sizes, Kevin brings skills in hardware, software, project management, technical communications, and organizational management. Well-known in Silicon Valley, he has worked as an engineering team lead, engineering manager, and executive at many high tech companies including Tandem, IBM, and Cisco. He has founded six startup high technology companies, including Force10 Networks, Mistletoe Technologies, and Violin Memory.

Ilya Teplitsky. Hardware Design Consultant. Ilya has over 20 years of hardware chip, board, and system level experience designing high-speed infrastructure-related products and technologies. Ilya held various positions at senior and management levels at start-ups (inSillcon, Alloptic), as well as larger companies, including Intel, Cisco, and Lockheed Martin. He is the co-founder and CTO of Rucka Inc, a healthcare wearable product company.

1 Introduction

Solving serial link Signal Integrity (SI) primarily involves resolving loss and discontinuities [1, Chapter 2]. Similarly, writing serial link specifications involves balancing the tension between loss and discontinuities. Specifically, what lengths, mediums, and modularity will work at a given data rate. Loss, or "insertion loss" (IL), in PCB-level interconnect attenuates a signal, and increases with increasing frequency and data rate. Discontinuities, or impedance changes within a physical connection, cause reflections that perturb SI and also increase with data rate (i.e., smaller features become relevant) – yet in a less predictable way than loss. As such, specifications, and hence the engineers that work with them, must increase data rate while keeping loss and discontinuities in check.

As PCI Express (PCIe) has increased data rates through each generation, the balance of loss and discontinuities has swung like a pendulum, as shown in Figure 1. While Gen1 forced a rapid introduction to differential-pair routing techniques, Gen2 taught us that PCB traces – as we knew them at the time – had measurable and significant IL to understand and overcome. As advanced equalization and dielectric materials arrived to alleviate our IL challenges, Gen3 and 4 data rates forced us to get our backdrilling and via impedances correct. Indeed, Gen4 represents the intersection of data rate, PCB dimensions, and discontinuities [1, Chapter 4]. With new discontinuities now understood and managed, Gen5's data rate doubling swings the pendulum back towards loss – as will be demonstrated.

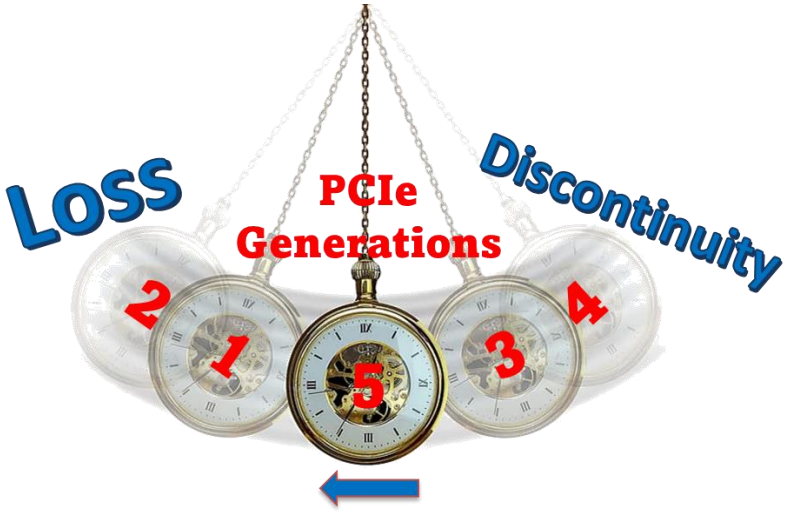


Figure 1: PCIe Generations, and their primary SI challenges

Due to its high-volume spectrum of products and implementations, PCIe has always stayed a few Gigabits-per-second (Gbps) behind its networking and disk drive standard counterparts. For example, PCIe entered the serial link world at 2.5 Gbps (Gen1) while established standards were at 3.125 Gbps. PCIe later advanced to 5 Gbps (Gen2) after the others figured out 6 Gbps, and then slinked back to 8 Gbps (Gen3) while the others doubled to 12 Gbps. Today, mainstream PCIe designs continue to grapple with 16 Gbps (Gen4) while the networking world confronts the complexities of 24 to 28 Gbps design.

In a rare move PCIe Gen5 endeavors to leap-frog industry data rates and push mainstream implementation to 32 Gbps. This jump, and other market forces, has caused one of the slowest adoptions the authors have experienced in decades. Nevertheless, there comes a day after the spec-writers and proof-of-concept demos are gone that the industry rises up and learns how to build systems using the new technology. And, thanks to a push from Artificial Intelligence (AI) applications and Compute Express Link™ (CXL), that day has come. CXL memory, now supported by all major CPU vendors and many others, is poised to benefit from Gen5's bandwidth and hence drive its adoption. That said, CXL is not only a faster connection but also represents a change in the relationship of memory to processors and processes [2].

Figure 2 shows an SI "Cheat Sheet" to illustrate how SI challenges and implementations have changed throughout serial link generations. To make the numbers more accessible and useful for other applications, some values are rounded off (e.g., Gen2 data rate shown as 4 Gbps). Values in this table will be described in subsequent sections and are fully detailed in the sections of [1] as indicated in the right-most column, and further presented in [3].

Signal Integrity Cheat Sheet

Feature	4 Gbps	8 Gbps	16 Gbps	32 Gbps	Unit	SIiP Section
Industry/PCIe terminology	Gen2	Gen3	Gen4	Gen5		
Fundamental Frequency	2	4	8	16	GHz	
Relevant Feature Size	160	80	40	20	mils	4.1, 2.1, 4.x
what's that?	traces	vias	conn pads	everything		4.2, 4.3, 4.4
Max Stub	64	32	16	8	mils	2.5, 1.3.3
backdrills	none?	seq-lam	2 layers	per-layer		
P/N Matching, static	10	5	2	1	mils	2.3
P/N Matching, dynamic			10 in 1.5"	5 in 1"	mils	2.3, 2.4
Route Style	45°	45°	curved	curved		2.4
Diff-pair Spacing (XY/Z, min)	25	25	25	30	mils	5.3
Insertion Loss (max)	16	22	28	36	dB	2.2, 3.5
Min EQ: Tx_FFE/Rx_DFE taps, CTLE	1 / 0	2 / 1, C	2 / 2, C	2 / 3, C	#taps	3.3, 3.4, 2.7
Length match method	serpentines		irregular spaced bumps			2.4
Fiberglass weave	spread glass and rotate image 12 degrees on panel					2.6
GND Return Vias (GRVs)	within 30 mils of signal layer transition (see DesCon 2022)					Figure 17
Solid GND reference layers	both sides of trace (don't use microstrips)					2.3, 2.6

To avoid crosstalk

Figure 2: Signal Integrity "Cheat Sheet," by generations

As Figure 2 suggests, the Gen5 SI challenges are substantial, often non-intuitive, and yet real. Overcoming them is the subject of this paper. Here we append to the issues and solutions of the previous generations [4] the new issues required to implement Gen5 and/or any serial link faster than 30 Gbps. To avoid offering unsubstantiated opinions, guidance and conclusions are substantiated by simulation as confirmed by physical measurement throughout. We begin, as intimated by Figure 1, with a discussion of loss.

2 Loss

2.1 Loss Budgeting

Given its 16 GHz fundamental frequency, PCIe Gen5 challenges our ability to manage insertion loss (IL) with today's materials and methods – even given Gen5's substantial and unprecedented system IL "budget" of 36 dB [5, Table 8-8, Note 2]. Because loss concerns dominate Gen5 connections, the first step in any implementation is to perform a simple IL summation for anticipated connection scenarios and generate a Loss Budget. To facilitate this, the four left-most columns in Table 1 approximate IL for common Gen5 system components – conveniently in terms of "eights". These components are then summed into common connection paths in the seven right-most columns. Note that, because certain connections require additional route length, route IL is doubled in some interconnect scenarios as appropriate.

#	System Component	IL (dB)	Notes	MB IC	MB AIC	AIC Cage	SSD Cage	Retimer!	to Rt	from Rt
1	Host/Switch IC	8	8.4 dB, [3] Figure 8-53	8	8	8	8	8	8	
2	Motherboard Route	8	~5" of trace, plus 2 vias	16	16	8	8	16	16	
3	1 Meter Cable	8	Includes mated connectors			8		8		8
4	0.5 Meter Cable	4	Includes mated connectors				4			
5	Adaptor PCB	4	Route conn to SSD/AIC slot			4	8	8		8
6	Non-Root IC	4	4.2 dB, [5] Figure 8-57	4					4	4
7	Add-in Card (AIC)/SSD	8	9.5 dB, [6] section 4.7.11		8	8	8	8		8
			IL Budget Totals (dB):	28	32	36	36	**48**	28	28

Table 1: PCIe Gen5 IL "Table of Eights" and Loss Budget Examples

Table 1 illustrates that even the simplest connection from a Host (or "Root") IC to another ("Non-Root") IC on the same Motherboard (MB) often consumes 28 dB (column "MB IC"). Indeed, around 10 dB – a substantial amount of loss in a Gen1/2 connection – is required to simply exit the Host IC. Because longer routes are required to reach an Add-in Card (AIC) connector on a motherboard, the next column sums 32 dB to implement an on-board AIC ("MB AIC"). More complex systems, such as those implementing Artificial Intelligence (AI), might require cabling to a nearby "cage" of AICs or Solid State Drives (SSDs). Mechanically, these cables and cages require differing cable lengths and widths, easily summing to the Gen5 maximum of 36 dB (columns "AIC Cage" and "SSD Cage"). Finally, most systems need connections that exceed the maximum IL (see column "Retimer!") and hence require inserting a Retimer (Rt) in the path. Note that adding a Retimer in the center of a failing scenario (prior to the 1-meter cable, per columns "to Rt" and "from Rt") does not divide the excessive IL (48 dB, in this case) in half due to the IL associated with the Retimer device itself.

In practice, because Gen5 system interconnects are generally IL-constrained and hence IL-linear, the simple summations shown in Table 1 work quite well. To illustrate this, simulated IL in Figure 3 (left) confirms that items 1, 2, 3, and 7 in Table 1 are approximately 8 dB. Combining these elements to simulate IL for system scenarios/columns "MB IC" (green) and "AIC Cage" (black) yields the anticipated sums of 28 and 36 dB respectively. A TDR of both scenario's impedance discontinuities *as viewed from the Rx* (right, same colors) reveals that even though all system segments are visible, and hence non-ideal, the significant amount of IL damps these discontinuities to allow linear summation. Even though a small amount of non-linearity can be

seen in the IL plots (left), this type of loss budget summation generally works well for Gen5 systems.

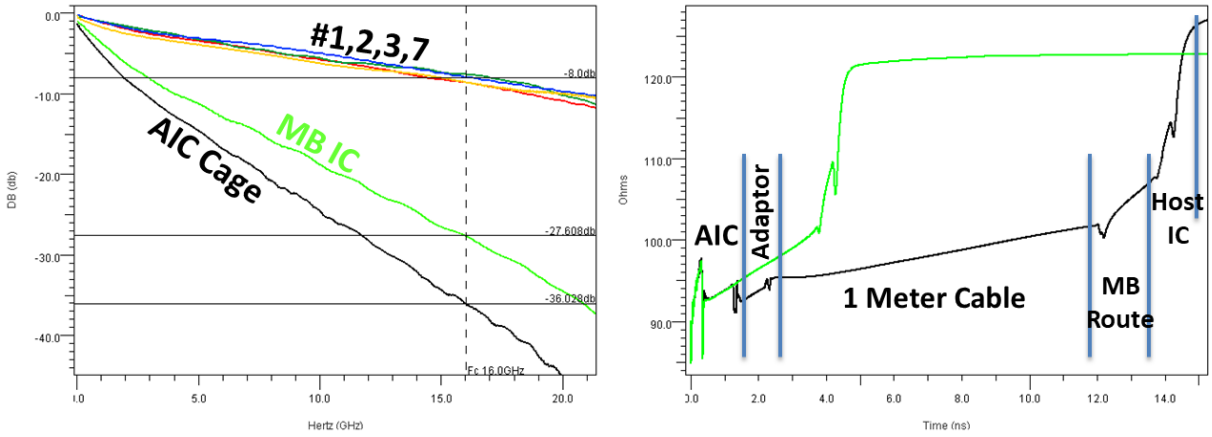


Figure 3: Simulations of Gen5 Loss Budget Scenarios

One interesting fact seen in Figure 3's TDR is that, per Table 1, *each delineated segment has the same IL* (with the exception of "Adaptor" which has half the IL of the others). That noted, it should be obvious that *cables, rather than PCB, are the best way to achieve distance* when IL limits, system modularity, and reach might require it.

This section has presented an efficient, albeit approximate, method to quickly qualify a variety of Gen5 system configurations. While IC IL might be a parameter that cannot be adapted by a system designer, IL of cables and PCB traces *is* a variable that can be controlled. However, be advised that at this frequency and stage of Gen5 adoption, *it can be quite challenging to get accurate and reliable IL values for both Gen5 cables and PCB traces*. As such, while the values in Table 1 seem tidy – and they are – this has required many man-months of measurement, simulation, and vendor iteration to derive and qualify the IL values shown. Hopefully by the time readers internalize this paper and implement the aspects described, it will be simpler to obtain reliable data. In the meantime, test, qualify and validate all data obtained from vendors, simulations, and measurement tools.

Implementing Gen5 systems in practice, cables and traces bring both good news and bad news, respectively, as detailed in the next two sections. We begin with the bad news.

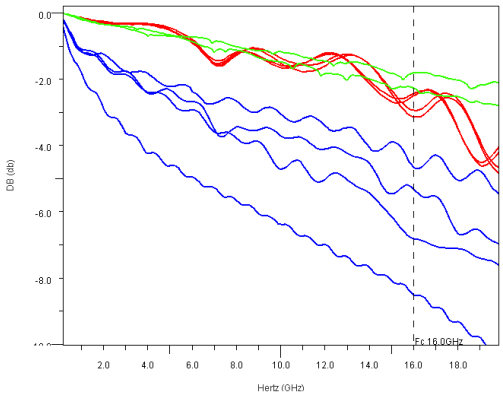
2.2 Gen5 PCB IL Challenges

A significant Gen5 challenge is achieving IL better than 1.5 dB/inch at 16 GHz using available and affordable materials – even with 6 mil wide traces. There are a few reasons for this:

1. **Materials**. Although the previous decade has brought an affordable 10x reduction in dielectric loss using newer materials (e.g., Df/Lt of 0.02+ for FR4 to 0.002 for Tachyon 100G and similar), this trend is not likely to continue. Though data rates continue to advance, PCB material Df is not expected to save the day as it did for Gen3 and Gen4. As will be shown, it is cabling that provides the next 10x reduction in IL per length.

2. **Higher Frequency**. While this is obvious, traveling further down the IL plot brings us face to face with issues we could ignore previously – specifically the next three items.
3. **Measurement**. The previous decade has also brought higher bandwidth measurement tools, specifically the Vector Network Analyzer's (VNA's) advance from 20 to 40, and 67 GHz. A natural outcome of increased bandwidth is the ability to observe and quantify effects that had not been accessible previously. Relevant to this discussion, measuring IL using 20 GHz VNAs showed less IL than we are seeing using 40 and 67 GHz equipment. This change is due not only to bandwidth, but also to changes in the way the new/old VNAs are used and calibrated.
4. **Simulation**. The above shift in measured data implies the so-called "golden" measured data we had previously used to correlate our simulators renders our simulations optimistic (i.e., likely to show less IL than actual). Additionally, the frequency-dependent effects of both dielectrics and conductors must now be characterized and modeled correctly, even though data for the same is not always available. These two problems have brought us, once again, to the necessity of correlating and re-calibrating our simulation environments. This is particularly true in regard to the next item.
5. **Conductor Roughness**. To avoid excessive conductor/copper loss at Gen5 frequencies, smoothness of copper must now be specified. Common terms for grades of copper are HVLP, HVLP2, HVLP3, and so on. The correct copper choice for Gen5 becomes a performance, cost, and material availability question. The selection challenge is further exacerbated by the fact that the industry lacka a proven/standard solution for characterizing and modeling conductor roughness [7]. This issue is acutely seen in the next item.
6. **Microstrips**. Gen5 brings us to the end of the use of microstrips, for a myriad of reasons. Perhaps the greatest of these is the fact that *to solder components reliably, outer-layer copper must be intentionally "rough"* – typically an order of magnitude rougher than is acceptable for Gen5 signals. And this roughness causes Gen5 microstrip IL to be ~3x higher than might be expected. Other previously noted issues [1, page 104] include the challenge of manufacturing a reliable impedance given the tolerance of pre-preg and soldermask surrounding microstrips [4, Table 3 and Figure 24]. While short microstrip routes (~50 mils) might still be used to connect component pads to AC capacitors, use of longer microstrip routes should be avoided.

To illustrate point #6 above, Figure 4 shows measured microstrip routes from 3 PCBs (left) along with their Fitted Attenuation (OIF algorithm, to linearize IL) IL "FA IL" and lengths (right). This data is formed into a dB/inch value at 16 GHz that is compared with a published reference value for stripline traces in the stated material [8 Figure 4, 9 Slide 63] to quantify how much greater microstrip loss was found to be (x Factor column). As shown, microstrip loss is generally two to three times greater than stripline – a difference we believe to be due to both excessive copper roughness and the higher Df found in soldermask.



PCB / Signal	FA IL (dB)	Len (in)	dB/in	Ref	x Factor
FR408HR / 1	2.60	0.68	3.8	1.33	2.9
FR408HR / 2	2.56	0.62	4.1	1.33	3.1
FR408HR / 3	2.57	0.68	3.8	1.33	2.8
FR408HR / 4	2.45	0.62	4.0	1.33	3.0
FR408HR / 1	5.68	2.0	2.8	1.33	2.1
FR408HR / 2	6.36	2.1	3.0	1.33	2.3
FR408HR / 3	9.00	4.0	2.2	1.33	1.7
FR408HR / 4	4.41	1.8	2.4	1.33	1.8
Tachyon 100G / 1	1.83	1.07	1.7	0.85	2.0
Tachyon 100G / 2	2.29	1.35	1.7	0.85	2.0

Figure 4: Measured Microstrip IL Across Three PCBs

To interpret the data in Figure 4 properly, a few items are worth noting:

a. Fitted Attenuation tends to average IL whereas, at least for the repetitive oscillations, it may be more accurate to derive IL from the peaks. Furthermore, discontinuities (primarily in the FR408HR PCBs) cause IL to be non-linear. These effects may cause the data to perhaps show a greater IL than actual.
b. Some of the signals have a via or pads on the ends. These features do have their own IL, which is not subtracted here. This may cause the longer lengths to yield lower factors, and that is somewhat true.
c. If copper was equivalent, microstrip *should* have less IL than stripline because one side of the trace is close to or in air, which has a low Df of zero. While the FR408HR PCBs had a thin soldermask, the Tachyon traces did not and hence were surrounded by air on all sides except the bottom. This implies IL is coming from an unplanned source, which is likely roughness.
d. Trace width is also relevant for conductor loss [10, Figure 2]. The blue PCB used 4 mil traces, the red was 6 mil, and the Tachyon PCB traces were 11 mils wide. As such, trace width is most relevant for the blue PCB.

We have found that even the shortest Gen5 routes cannot be implemented in microstrip - regardless of material Df. This is disappointing, as it can be desirable to use microstrip for small/simple PCBs with few layers and/or to remove stubs. Per Table 1, it is generally not acceptable in the larger system for a 0.7" PCB route to consume 2.5 dB, or a short 2" route to consume 6 dB. As such, many microstrip routes that may have been acceptable in previous generations must migrate to stripline.

While it would be excellent to find a good low-loss Gen5 PCB trace solution, after dozens of measurements across numerous implementation ideas and materials, *we have not yet found a single implementation or measurement that provides an IL as low as we had hoped for*. As such, we believe Gen5 PCB routes must be implemented and budgeted as follows:

i. Avoid microstrip and use stripline traces with widths of 6 mils or greater.
ii. Clearly specify and use HVLP2 copper or better.
iii. Use materials with a Df from 0.002 to 0.004 at 16 GHz and expect to achieve 1.2 to 1.5 dB/inch at 16 GHz from the same.

This data explains why Table 1 budgets 8 dB for 5” of PCB trace. Indeed, with IL accumulating so quickly in PCB traces, we have found that it is often best to breakout from ICs and route to a cable connector as quickly as possible. In our system (Figure 5), due to over 500 Gen5 diff-pairs emanating from a single BGA, we have found that PCB traces require ~5” routing to reach a connector – based on two Tx and two Rx breakout layers and space for heatsink mechanicals (that block cable insertion - heatstink is not installed in Figure 5, though mounting holes are visible).

Figure 5: PCIe Gen5 Component’s relationship to connectors

Given the difficulty of implementing low-loss PCB routes, the next section details our cable IL findings – largely good news against the PCB IL challenges described above.

2.3 Cables to the Rescue

Cable measurements reveal IL at 16 GHz of ~0.06 dB/cm (0.15 dB/inch) – which is 10x less than PCB routes. IL measurements shown in Figure 6 were performed on 36 cable configurations spanning four vendors (designated by colors: red, gold, blue, green) and four lengths (0.25m, 0.5m, 0.75m, 1.0m). The cables measured here are Gen5 “MCIO” cables with vertical connectors on each end. Note that each vendor did not provide all four lengths (e.g., “Blue” vendor provided 0.25m, 0.5m, and 0.75m cables, “Red” vendor provided only 0.5m). Because measurement equipment, fixturing, and data post-processing is complex with various uncertainties, the data is presented two ways: IL extracted from raw/non-linear plots (left), and IL linearized using an OIF CEI 4.0 Fitted Attenuation (FA) polynomial (right). IL values are extracted from each data set at Gen5’s 16 GHz fundamental frequency (black vertical dashed line).

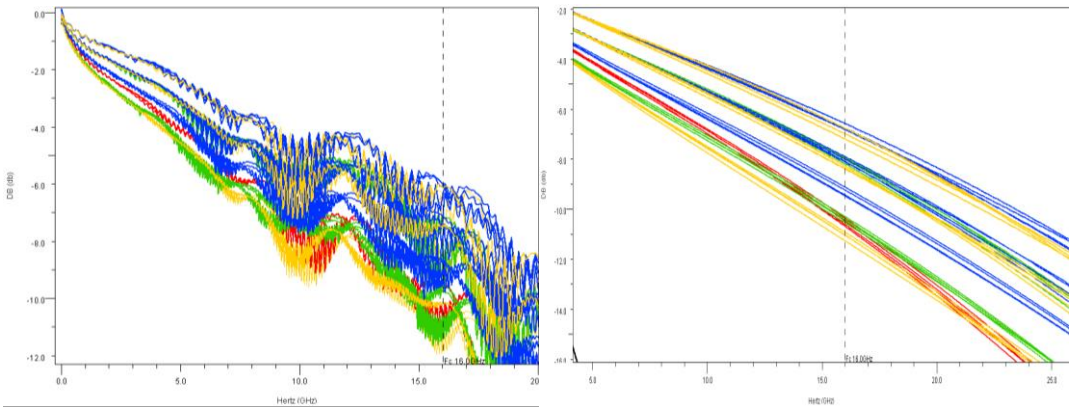


Figure 6: MCIO Cable Measured IL, raw (left) and linearized (right)

The data extracted from Figure 6 is processed, organized, and plotted in Figure 7 – both raw (upper) and linearized (lower). Cable length is increasing from left to right (0.25m, 0.5m, 0.75m, 1.0m, marked as 2, 5, 7, 1, respectively), and vendors are delineated by color on the X axes.

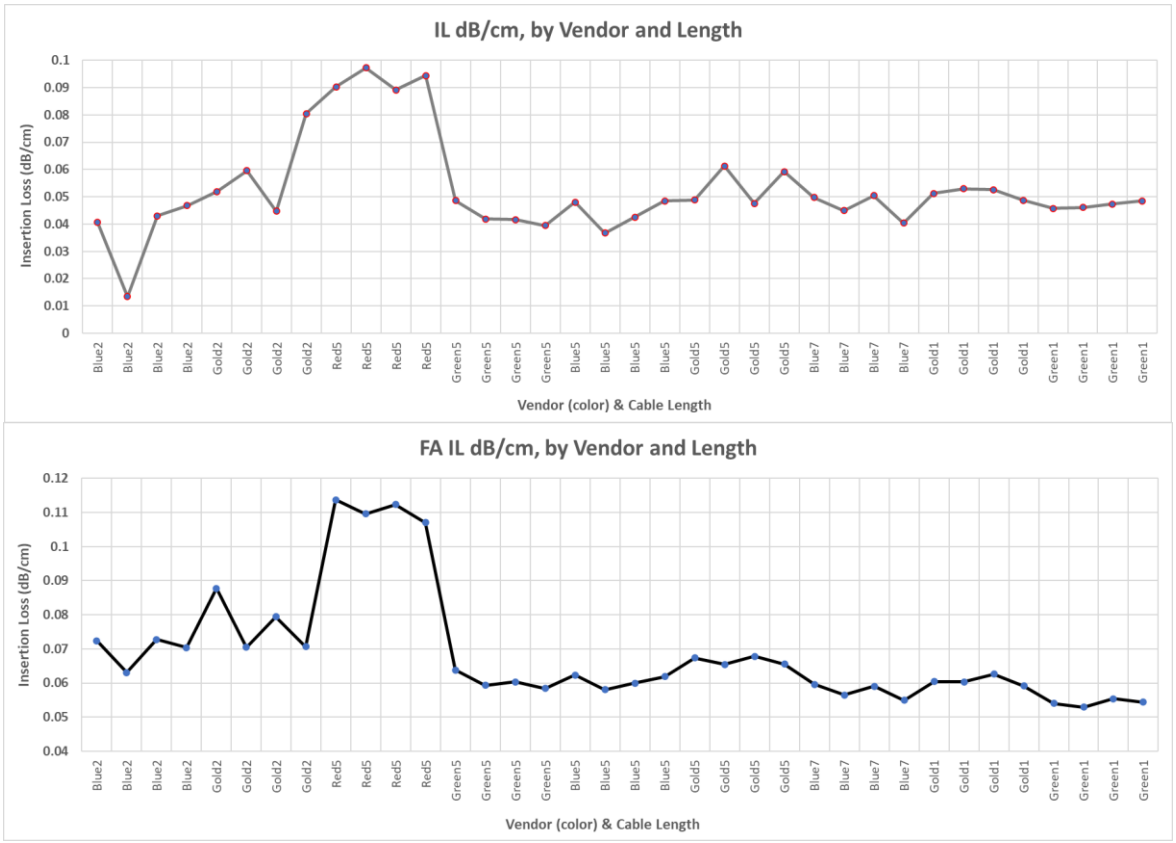


Figure 7: MCIO Cable Loss, 36 Measurements

Observations from Figure 7 plots and data are:

1. "Red" vendor's IL is roughly twice the value of the other three vendors. As these were the first cables received, updated cables were requested from this vendor yet have not been delivered as of this writing. As such this vendor will not be used. To avoid a similar problem, the reader should request models and/or characterization data from vendors to verify performance.
2. Due to lower IL of the shorter 0.25m cables, and though methods were attempted to remove the effect of the mated connectors, the data is more erratic. In contrast, the data becomes more linear as cable length increases. Nevertheless, fairly consistent IL is seen when ignoring a couple outlier 0.25m data points.
3. For the same length, as seen in both Figure 6 and Figure 7, blue vendor's IL is lower than gold's. As might be expected, cable IL varies by lot and by vendor.
4. The fitted attenuation (FA) method produced higher IL values than the raw data method. It is reasonable to view the FA data as conservative, as some, but not all, of the ringing in the raw IL plots is VSWR-induced which deterministically reduces IL. Hence, where this occurs, correct IL is found at the top of the ringing while the FA algorithm trends IL towards the center of the ringing.

5. Depending somewhat on vendor and length chosen, and ignoring the red vendor, **MCIO cable IL is approximately 0.06 dB/cm**. As stated previously, this is **0.15 dB/inch** or 10x less loss than measured in PCB traces as detailed in the previous section. Based on this value, a 1 meter cable and its mated connectors are shown to have 8 dB IL in Table 1. Though we've been unable to think this way previously, when picturing Gen5 connections, consider viewing 2" of PCB route to have IL similar to 20" of cable.

Our conclusion and assertion that, when length is needed in a Gen5 connection, it is better to use cable than PCB is based on this measured data and is further confirmed by new vendor models starting to become available. Additional impedance and time delay data measured from the cables will be shown in the section on discontinuities further below.

2.4 Gen5 Equalization Improvements

Even when attempting to minimize lengths of PCB traces and cables, we have found 31 dB to be the average IL of the many system connection scenarios we must handle in practice (with a standard deviation of 6 dB). Realizing these higher IL connections would be inevitable, PCIe spec writers continue to increase Tx and Rx equalization (EQ) expectations – baseline capability that component and SerDes vendors typically exceed.

Figure 8 is a simulation of our SerDes handling a channel with an IL beyond the spec's assumption of 36 dB, revealing the Rx EQ's ability to recover data (red) from a signal at the input to the Rx (blue). While the eye of the signal arriving at the die (blue) is obviously closed, EQ properly detects a change in signal level (red) from the slightest change in the incoming signal's slope (blue) – thus compensating for a channel that delivered only 1% of the Tx' signal and opening the eye. While many SerDes offer "eyescan" plots of post-EQ eye openings, this type of waveform can typically only be derived using IBIS-AMI simulation of the system.

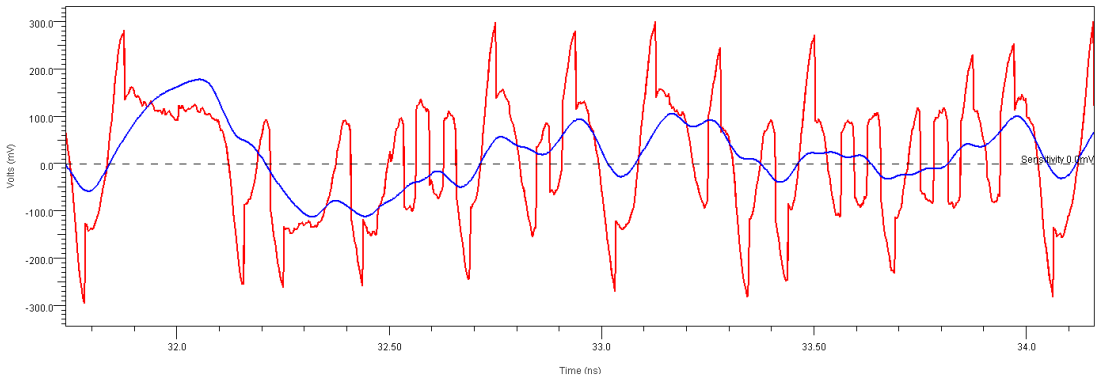


Figure 8: Rx equalization recovering a valid signal (red) from its input (blue)

Though Gen5 system's higher IL tends to dampen the effects of discontinuities, Figure 8 reveals how EQ makes signal-level decisions from the slightest change in signal slope. As such, it remains imperative to minimize Gen5 system discontinuities to ensure these slope changes were injected by the Tx and were not due to a reflection caused by a discontinuity. Indeed, Gen5's data rate not only makes handling IL challenging, but also causes nearly every structure on a PCB to become a discontinuity.

3 Everything is a Discontinuity

A simple rule-of-thumb, used in Figure 2, to determine which features are large enough to disturb a signal based on data rate is:

Relevant Feature Size (RFS) ~= 0.6*UI(ps) mils [11]

In other words, 60% of the UI gives the RFS in mils. As such Gen5's RFS is 18 mils, which includes just about everything - BGA pads, connector pads, backdrilled vias, and so on. As such, we now need to solve and manipulate the impedance of every feature in our PCB layout to ensure it matches the impedance of the features next to it so it does not present a discontinuity and hence signal reflection. This section will explore the implications of this small Gen5 RFS and provide examples and solutions for addressing it.

3.1 What, that's a stub?

The maximum Gen5 stub length is half the RFS, or 9 mils (=0.3/32 Gbps [12, slide 5]). As such, *Gen5 requires per-layer backdrilling,* or backdrill depths that target every Gen5 signal layer such that, given drill tolerance, the maximum via stub is less than 9 mils. While that's now common in PCB fabrication, what's not so simple is eliminating "stubs" we didn't have to think about previously.

Figure 9 shows a number of features that now behave as stubs (red rectangles). While the top item (a backdrilled via) is understood, most are not accustomed to thinking of the other items shown as stubs. The second item illustrates that *signals must route into connector pads at the end opposite the connector solder leg exit.* Failing to get this correct has been shown to significantly increase Gen5 Bit Error Rate (BER). Said another way, if you route from the back side of the connector pad (from the right side in Figure 9), the signal's energy will be split between the connector leg and the ~50 mil "stub" which is the connector pad. And 50 mils is too long for even a Gen3 stub (Figure 2), and hence is unacceptable at Gen5.

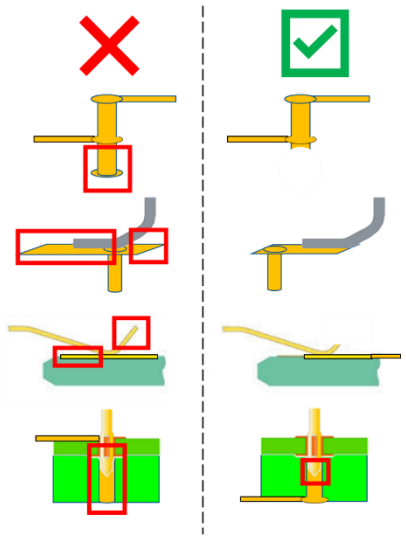


Figure 9: Hidden Gen5 "Stubs" (red rectangles), and how to remove them

The lower two items in Figure 9 (edge-finger connector wipes and press-fit pins) are largely the responsibility of the connector vendor and specification to resolve, respectively. However, they do provide examples of structures larger than 9 mils that must be understood and eliminated. The press-fit pin example illustrates why 25+ Gbps serial standards now require surface mount connectors.

3.2 Discontinuities in a Gen5 signal path

Armed with the RFS and maximum stub length we now travel down the signal path from Tx to Rx, discovering all potential discontinuities along the way. Figure 10 shows a typical set of system elements that must be impedance matched so they do not cause a discontinuity and hence signal reflections. In the sub-sections that follow, we'll discuss these items individually. However, as the colors suggest, it can be helpful to comprehend and solve each item in light of the elements that are on either side of it – particularly if that item is "short" relative to the RFS.

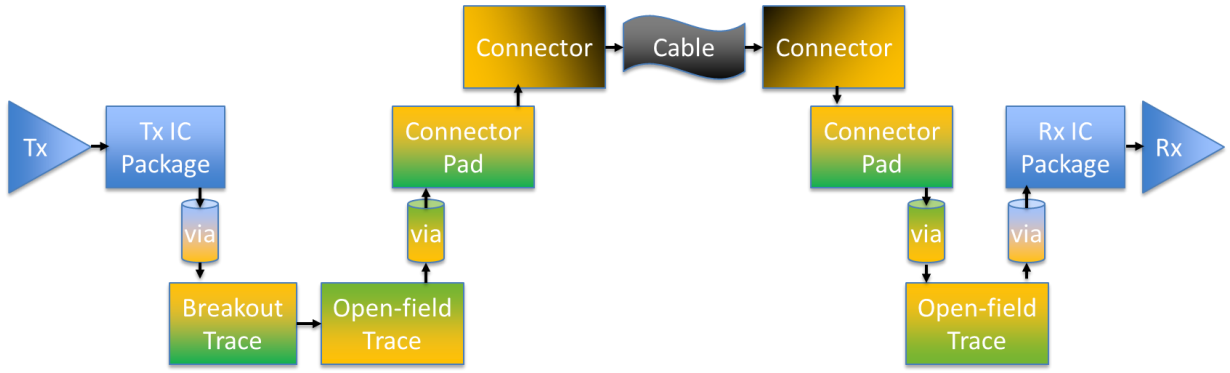


Figure 10: Typical set of discontinuities in a Gen5 Tx to Rx path

3.2.1 Getting off the IC

If you are purchasing ICs, the characteristics of the IC package may be out of your control. If so, be sure to request S-parameter models for your IC packages and confirm they satisfy the items below. If you are designing an IC, you should influence your package design to achieve these same items.

a) IL is within specification limits, per Table 1.
b) There is no p/n skew. This is confirmed by converting the S-parameters to single-ended TDT, and plotting/comparing the through paths in time. If you find a mid-voltage swing p/n skew greater than 1 ps, bring it to the attention of your IC vendor for correction. It may be a problem in the S-parameter model or in the IC itself. While DDRx layouts have often compensated for miss-matched package skews on the PCB, this practice is not done for serial links – particularly at Gen5. It is the IC vendor's responsibility to ensure the signal delivered to the PCB does not have p/n skew.
c) Impedance is reasonably flat and bounded, as confirmed by examining the package model in TDR. The package route's differential impedance may be 85 or 100 Ohms, or something in between, and this may influence how you route to it on the PCB. Many ICs show a small impedance dip at the die and at the ball, and you may be able to

compensate for a dip at the ball on the PCB. Quantify how large any discontinuity in the package may be relative to the RFS and act accordingly.

When the package is understood, juxtapose its characteristics on top of the impedance stated for your Tx or Rx to understand what discontinuity might exist at the SerDes/package boundary.

3.2.2 Short Via-in-Pad

To manage the routing of hundreds of Gen5 signals, our team uses Via-in-Pad (ViP) style vias below the BGA balls. As shown in our ballmap in Figure 11, Tx signals (green) are placed towards the outside edge of the IC and use short ViPs while Rx signals (gold) are placed more to the center and use longer ViPs. Because the Tx signal's edge is the fastest in the path (on the order of 7 ps, or 0.20 UI), we damp it with the longer package IL and send it through a ViP that is less than the RFS. To breakout our signals, two Tx layers and two Rx layers are required, hence Tx via lengths are short at 9 and 18 mils while Rx via lengths are longer at 27 and 35 mils. The shorter Tx via lengths reduces the impact of any potential discontinuity due to fabrication tolerances. Vias are designed to be 85 Ohms [13] and measured to be about 87 Ohms (Figure 11, at right) on our first PCB fabrication. All vias use per-layer backdrilling to remove stubs.

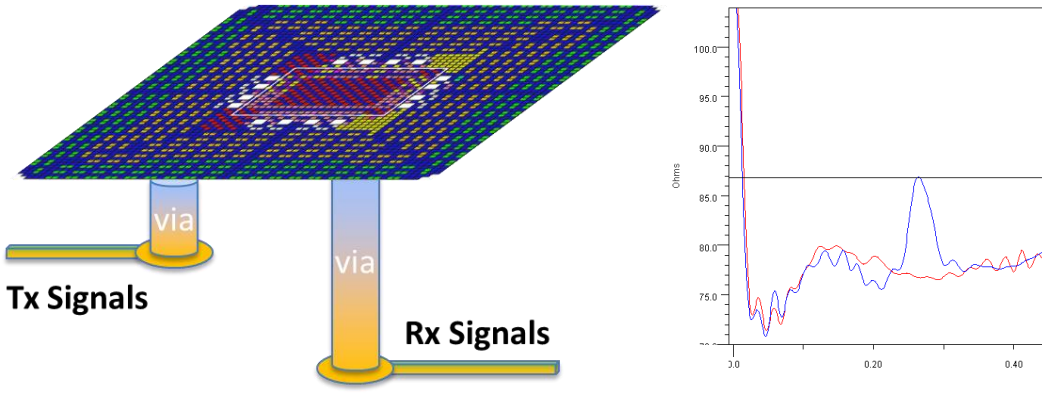


Figure 11: ViP orientation (left) and impedance (right)

Significant attention and mitigation was also applied to differential signal via crosstalk as a function of surrounding ground return vias (GRVs), as described in [14,15].

3.2.3 Breakout routing

Our breakout traces used 85 Ohm differential pairs (4.5/5.5 mil trace/space) between the BGA balls, using small pads and antipads to achieve clearance. Even though one side of the diff-pair often routed near more voids than the other, single-ended TDR measurement (not shown) revealed an acceptable p/n impedance match to less than 1 Ohm. Figure 12 is a differential TDR of eight breakout traces of varying lengths (breakout region for longest traces between black vertical lines). Due to hundreds of Gen5 signals in our IC, some breakout traces were ~1.5" long (red) yet did not show significant impedance variation when compared to signals leaving the edge of the IC (green) or mid-length routes (blue). At 25 mils pair-to-pair spacing under the BGA, crosstalk was found to be acceptable as well. Figure 12 reveals this PCB fabricated on the low side of impedance tolerance, and it also exhibits artificial mathematical conversion ringing at the bandwidth of the measurement device (40 GHz).

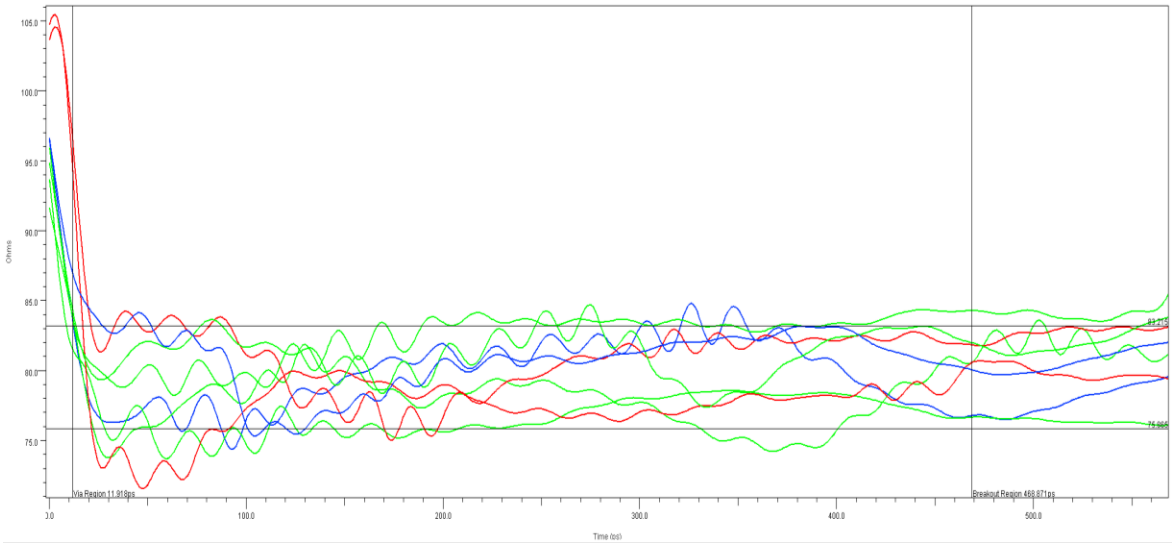


Figure 12: Differential impedance range and variation of breakout traces

3.2.4 Open-field PCB routes

While 2.5D solutions of trace impedance have been understood and correlated for many years, a couple open-field routing items must be noted:

1. Be sure your trace solutions and models are frequency-dependent versus Dk/Df, with trace impedances primarily referencing the highest fundamental frequency of 16 GHz.
2. To mitigate fiberglass weave issues, use only spread-glass dielectrics and rotate your PCB's image on the fabrication panel by ten to fifteen degrees [1, section 2.6].
3. To length-match p and n traces, stagger bumps that are smaller than the RFS at irregular spacing throughout the route according to the static and dynamic phase values in Figure 2.

To illustrate point number 3, we have known since [4, page 12] that tight repetitive length-match serpentine bumps cause substantial measured TDR single-ended and differential impedance variation (Figure 13, upper – 22 Ohm variation single-ended, differential variation somewhat masked by a high microstrip route of 90 Ohms). What is not intuitive is that spreading out more than twice the length-match bumps at irregular spacing does not cause measured single-ended or differential trace impedance variation (Figure 13 lower, see 100-300 ps region delineated by black vertical lines).

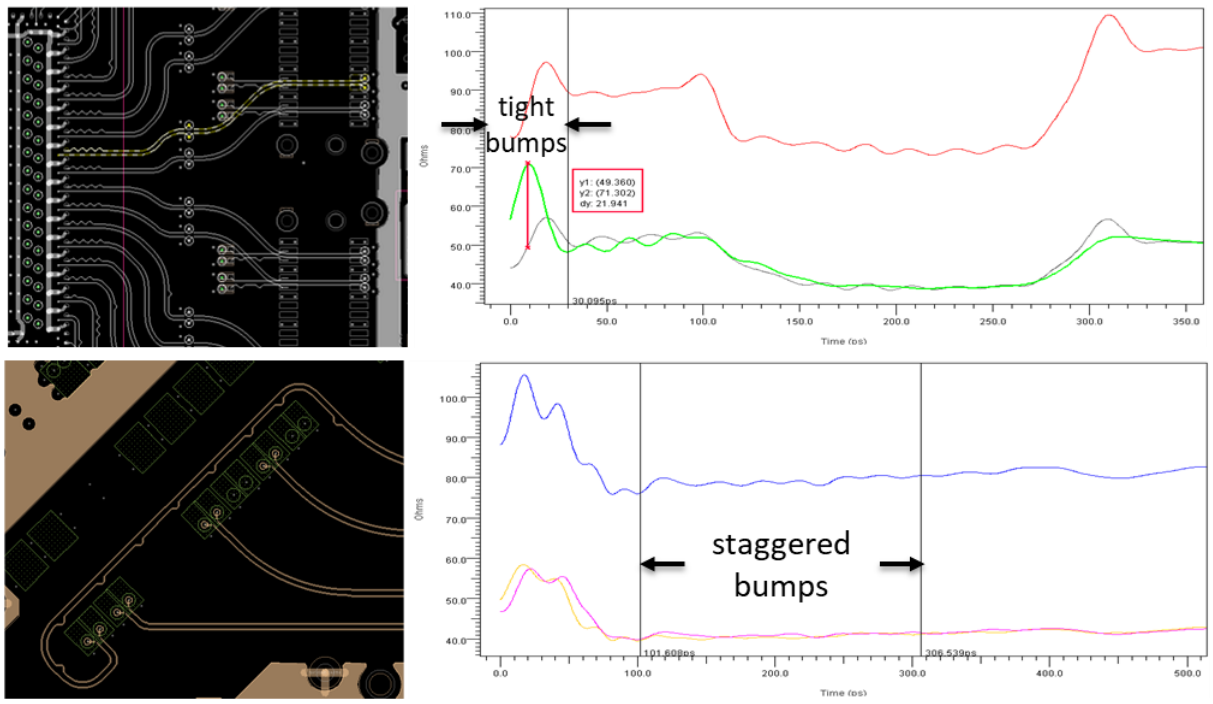


Figure 13: Correct (lower) and incorrect (upper) p/n length matching

3.2.5 Via into connector pad

At this point in implementation history, it goes without saying that only one via is allowed to connect the stripline open-field route to the connector pad, as shown in Figure 10. Furthermore, this via *must connect to the opposite end of the pad from the connector leg escape* as shown in Figure 9. These vias must also be 85 Ohms and backdrilled, similar to the vias at the BGA, as explained in [13]. Note that, should you choose *not* to backdrill a via to your lowest signal layer, Figure 14 demonstrates this via's "stub" is comprised of not only the via barrel but also the pads required to get to the end of the path. This can easily make this type of stub too long (e.g., 11 mils = 4 mils for pad ring + 3 mils for dielectric layer + 4 mils for bottom pad ring). While measurement shows this type of stub is detectable due to its length, each design team should assess the implications (cost/performance) of not backdrilling this stub.

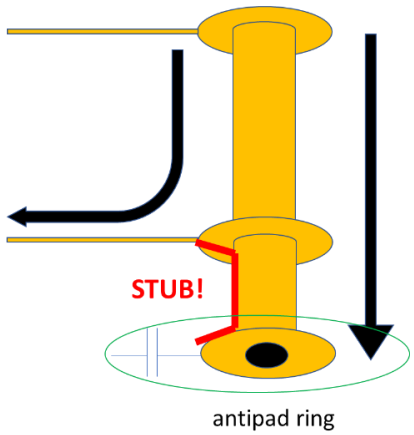


Figure 14: Stub lengths include pads, if not removed

3.2.6 Connector pads

Gen5 connector pads will range in size from 50 to 120 mils long, and hence are longer than the RFS and must be solved for proper impedance as follows:

1. As confirmed by measurement, we have found 2.5D trace solvers effective at solving the differential impedance of connector pads. Because connector pads are exposed to air, when using these solvers be sure they are set to "microstrip" and not "buried microstrip" (under a solder mask layer) as the impedance difference will be substantial.
2. Based on your stackup, your solver will likely show you options that are lower than 85 Ohms (due to wide pad width and ground referencing one layer down) or higher than 85 Ohms (due to voiding layers and referencing ground layers further below the pads). We recommend *not simply choosing the option that is closer to 85 Ohms* and instead implementing a partial void that splits the difference between the impedance solutions. In other words, it may be best to partially void a reference on layer 2 or 3 and then further reference a deeper layer. While this may sound complicated, it works surprisingly well for typical Gen5 PCB dimensions, as weighted by 2.5D trace impedance solutions.
3. When voiding under connector pads, *be sure to eliminate Z-direction (vertical) signal coupling* even between a signal on a lower layer and the connector pad itself. Per [16], this is the most common crosstalk issue and design-rule checks (DRCs) typically do not identify this problem. As shown in [16], only 30 mils of Z-direction coupling can shrink your eye by 30 mV – which may be all the Gen5 Rx eye margin you have.

3.2.7 Cable connectors

Cable connector models may come standalone (i.e., no cable connected) from your vendor or mated and embedded on both ends of your cable model. The items worth noting here are:

1. Not all connector/cable vendors are at the same point of sophistication (and hence impedance accuracy) in their physical devices and models, as described in [1, 4.4.1]. Furthermore, though they may have substantial expertise within their company, and you have learned to trust them, you may find this expertise is not transferred efficiently into their high-volume product lines – which Gen5 will soon become. As such, be sure to validate connector impedance using measurement, simulation, or both.
2. Connector vendors have long-played a "specsmanship" game when showing their measured and modeled impedances that severely limits bandwidth – sometimes with rise times beyond 50% of a UI. While this practice may be fair further down the channel towards the Rx where the edge rate has degraded, it is not reasonable closer to the Tx. As such be sure to either plot the TDR impedance of connectors with higher bandwidth or request better data from the connector vendor.
3. As with the IC package, be sure to examine single-ended TDT to verify the connector/cable's p/n skew is acceptable. If you find a p/n skew greater than 0.05 UI, request your vendor to provide a better model and/or improve their design.

Figure 15 shows that measurements of cable connector impedances (beyond fixture impedances, or to the right of 250 ps in the plots) across four vendors from both ends (left, right) reveal some vendor's impedance zones are notably worse than the others (Blue wipe, Green housing, and

Gold/Red attach). These impedances were measured in Q2 2022, and over time we expect connector vendors will characterize, study, and improve these items within their designs.

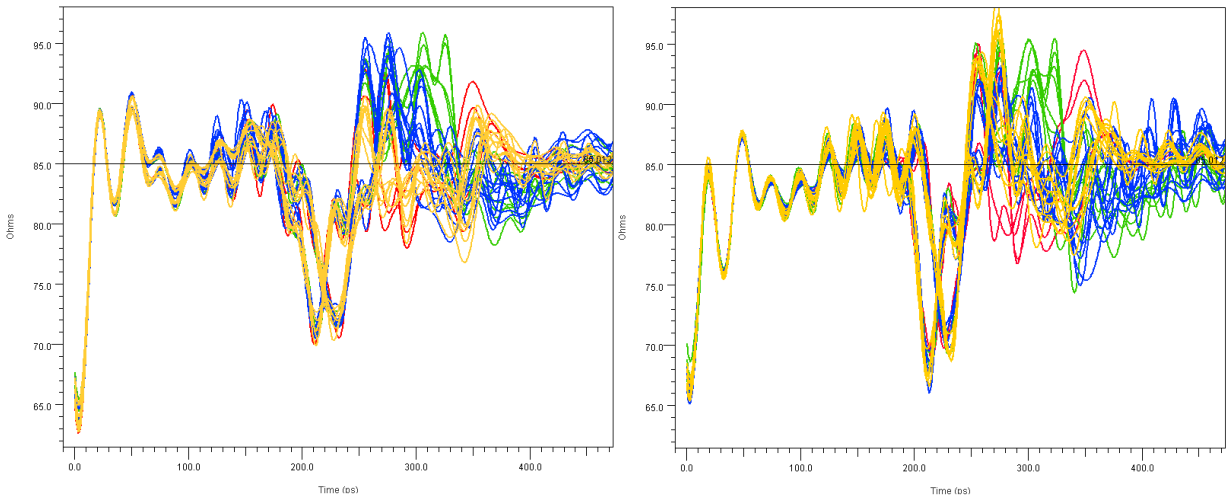


Figure 15: Cable connector impedance measurements, four vendors (by color)

3.2.8 Cables

Adding to MCIO cable IL plots shown across a sampling of four vendors and 36 cables in section 2.3, this section shows the discontinuities found in the same measurement set. Figure 16 shows both TDR (left) and TDT (right) for all cables, revealing a good impedance tolerance of 85 to 89 Ohms across all cables (left, horizontal black lines). Note that, due to non-ideal test fixture discontinuities, all four lengths (0.25m, 0.5m, 0.75m , and 1.0m) are visible with one vendor at the higher impedances and another at the low. TDT (right below) reveals a ~1.1ns difference between the 0.25m lengths, suggesting a signal propagation speed of 112 ps/in. With 2x that amount of variation in the 1m cables (far right), we see a difference of 2" between one vendor (short) and another vendor (long, or difference could be Er), which may explain that vendor's higher value IL/length in Figures 6 and 7. An almost 1" variation is seen in the sampling of 0.5m cables, with a third vendor ½" longer than all others (thus, the others are within ½"). Comparing 0.5m cables, and removing this inconsistent vendor, shows a 14 ps (~1/8") variation within each vendor's cables.

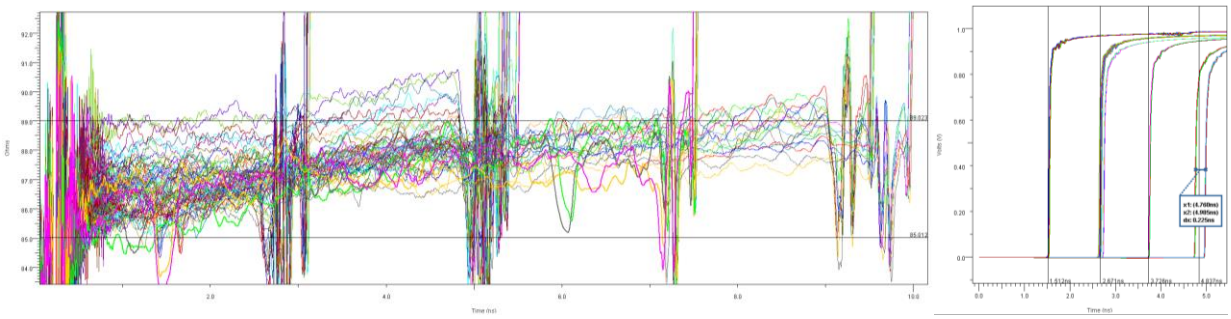


Figure 16: Cable impedance measurements, 36 cables in TDR (left) and TDT (right)

3.2.9 Completing the path to the Rx

As the remaining elements shown in Figure 10 are redundant with those previously described, this completes our explanation of the Tx to Rx path and the discontinuities therein.

3.3 Unexpected Discontinuities

While the previous sections articulated substantial, yet understandable and thus solvable, Gen5 path discontinuities, it's possible the most insidious of all discontinuities are the ones you did not expect. For example, Figure 17 shows a measured ~15 Ohm / 15 ps discontinuity in what otherwise would be a good and consistent 85 Ohm route. Here the discontinuity is caused by a 60 mil void (highlighted by the red circle) in the reference plane on one side of the trace. Indeed, field solution reveals removing this plane raises the differential impedance above 100 Ohms. This example reinforces the importance of detecting and correcting every feature larger than RFS (defined at the beginning of section 3 to be 18 mils), which, for this example, required additional per-layer visual vigilance during PCB layout review.

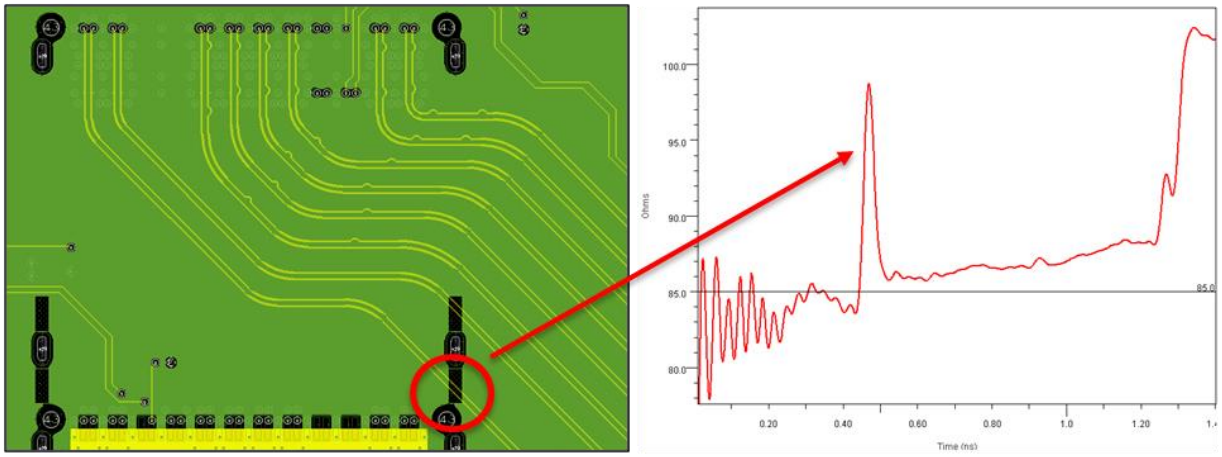


Figure 17: Unexpected Discontinuity due to Plane Cutout

4 System Issues

Given proper attention to component-level loss and discontinuities described in the previous two sections, Gen5 system-level performance is then examined and validated using a variety techniques and metrics, as discussed in the following sections:

a) Passive interconnect characteristics versus defined masks, simulated and/or measured.
b) Active interconnect performance versus eye opening, simulated and/or measured.
c) Hardware link performance, per Bit Error Rate (BER) and lab testing.

4.1 Passive Analysis

It is imperative to analyze passive performance in both minimum/short paths and maximum/long paths. Short, low-loss paths struggle to meet return loss masks (RL, measured from each end of a connection per [5, page 1037]) due to discontinuities and reflections. In contrast, longer high-loss paths struggle to meet the Gen5 insertion loss (IL) target of 36 dB. Here, we look at the minimum and maximum paths separately.

4.1.1 Minimum (Short) Paths and RL

One example of a problematic Gen5 minimum path is a short route to a Gen5 Add-in Card (AIC) connector. These may occur on the AIC itself, or from a non-root – and hence less-damped – device (e.g., a Retimer) placed near the connector on a motherboard or adaptor PCB. The characteristics of Gen5 connectors are not ideal and reflective. As such, placing an active device too close to it on either side (less than ~1.5 dB IL) will fail the RL mask. This can generally be fixed by using at least 2" (minimum) of routing to damp the signal between the device and the connector pad (see also [1, section 3.5]). Unfortunately, the CEM specification [6, 4.7.11] defines only a max IL and no minimum. Furthermore, use of the spec's AIC S-parameter model to simulate the path will not reveal this issue because it has a high IL. Figure 18 shows how simulating against the Gen5 RL mask causes violations at relevant frequencies (left) due to a 1" AIC route. Performance can be improved by increasing route length (center), while using the spec's AIC model (right) hides the problem. While adding IL/length to damp a short path is a non-intuitive solution, and should be verified to be within budget, it has been shown to be effective in numerous scenarios.

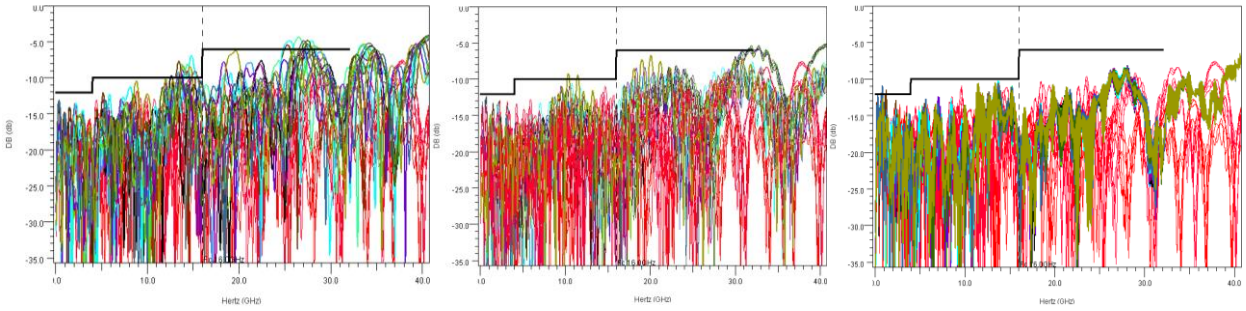


Figure 18: Using IL to damp reflections and meet RL mask

Another potential short path connects two active devices on the same PCB. As one device should be a higher loss "root" device, the signal should be well-damped from that end. However, RL when driving from the smaller-packaged device towards the root device's package balls should be tested and damped as appropriate.

4.1.2 Maximum (Long) Paths and IL

Per the many IL challenges described previously, Gen5 designs will typically be confronted with a variety of high-loss paths. Our highest loss paths involve multiple connections that cable to an AIC backplane. Figure 19 shows the simulated linear characteristics of this 35 dB IL (red) connection, agreeing with Table 1's "AIC Cage" estimate of 36 dB for this type of path. While this connection has numerous discontinuities, the path is IL-dominate (i.e., IL is the primary challenge to solve) as RL (green/grey) stays well below 15 dB. The channel's unequalized pulse response (blue) reveals significant spreading into neighboring UIs, with 1+ mV noise out to 10 pre-cursors and 40 post-cursors. Applying spec-level EQ (Tx=P8, Rx=3-tap_DFE and CTLEs self-adapting), the equalized pulse response (gold) removes much of the ISI – at the expense of amplitude [17]. Challenging borderline cases such as this must be additionally analyzed using active analysis, as described in the next section.

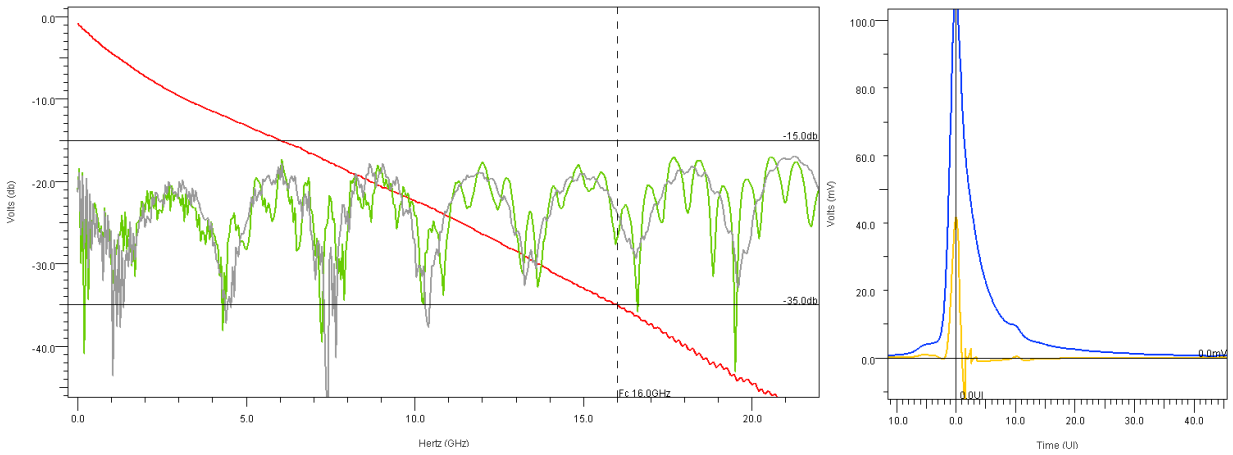


Figure 19: Maximum IL Path Characteristics

4.2 Active Analysis

While conformance to passive masks offers one Gen5 compliance metric, PCIe has asserted since Gen1 that eye diagrams represent a more reliable measure of system performance. As such, this section examines eye openings in our maximum IL channel shown in Figure 19, using both Gen5 reference Rx equalization (EQ) as contrasted with the EQ available in our component. Because most components provide EQ well-beyond spec requirements, the performance difference quantified here is typical of many scenarios.

Figure 20 demonstrates how Rx EQ recovers a signal from a signal applied to the Rx input (black). As the signal (black) wanders above and below 0V, its eye opening is closed. Here Tx EQ (P8, or 3.5 dB pre-cursor and 3.5 dB post-cursor) is applied to the same channel, with two different self-adapting Rx EQ solutions at the far end: (1) PCIe Gen5 spec reference Rx EQ (red), and (2) the more advanced Rx EQ provided by our IC (green). While both Rx EQ options recover an eye, our IC (green) shows substantially more amplitude.

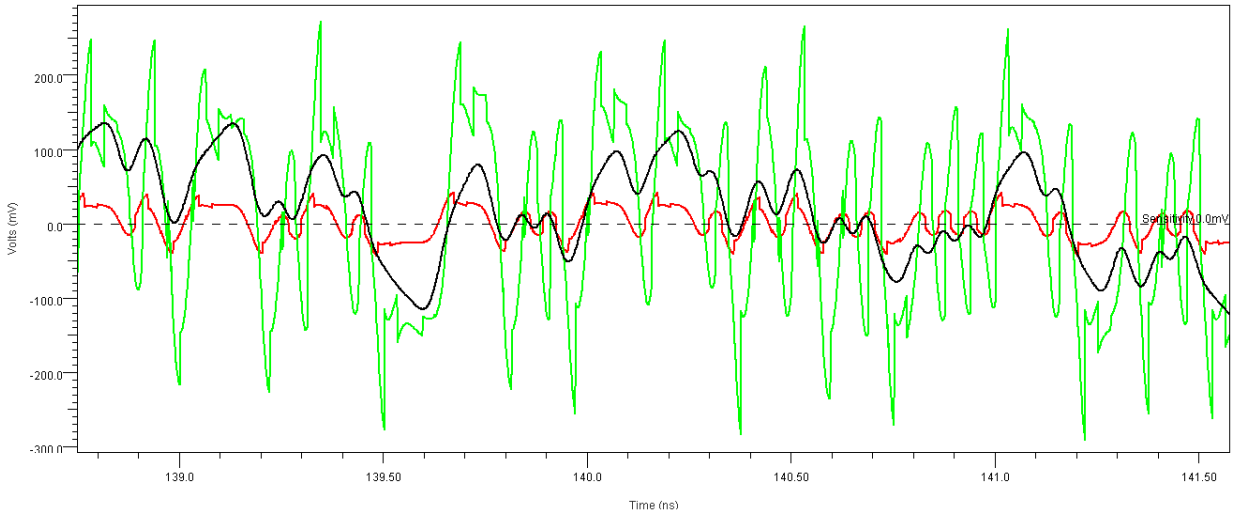


Figure 20: Rx input (black) applied to spec EQ (red) and Xconn IC (green)

Eye diagrams shown in Figure 21 reveal our equalization yields an eye height (left) that is six times larger than spec EQ (right). Though both eyes are "open," it is important to note that the Y scale is 6x larger at (left) compared to (right), or 600 mV compared to 100 mV, and that the spec eye masks (black) are the same. Eye heights are also 6x larger, or 91 mV (left) compared to 15 mV (right). While we would hope and expect a 36 dB channel passes the spec's eye mask (black) with reference EQ, at some probability/BER (see inset statistical plot, lower right, darkest blue is 1e-45, light blue is 3e-8) the reference EQ begins to fail.

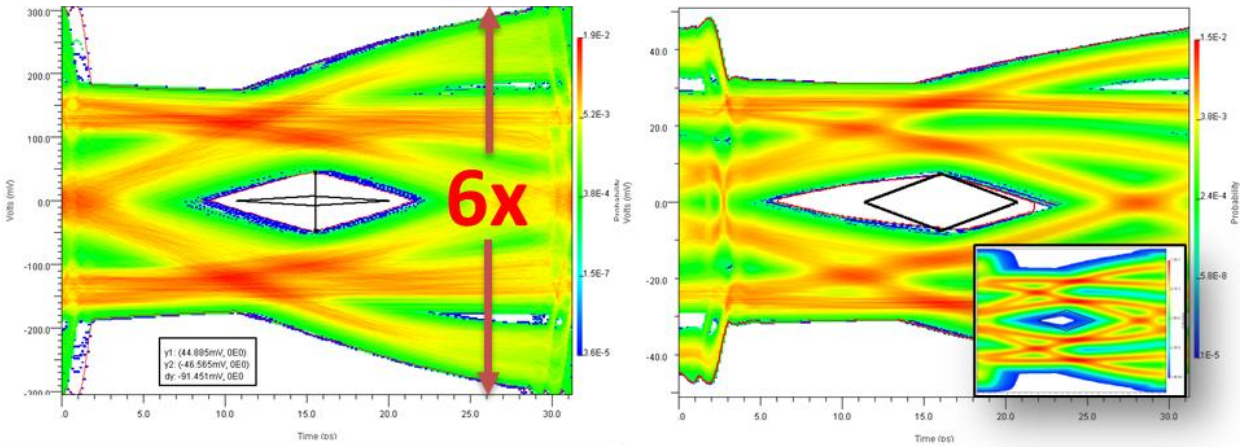


Figure 21: Eye diagrams, Xconn IC (left) and Reference (right) EQ

Figures 20 and 21 illustrate how system-level margin may change when contrasting Gen5's minimum-required EQ with EQ found in a Gen5 component. In the scenario examined here, a myriad of Rx EQ options might exist at the AIC end of the channel, so it is helpful to quantify the performance seen at that end using models of anticipated devices.

4.3 System Component Design Considerations

This section uses insights and observations from previous sections to highlight design considerations for various components in the system:

1. **Host/Root IC.** Though the spec allows significant IL in the package, effort to reduce/minimize IL can help downstream implementation. Given host IC size, this is often difficult to achieve. Nevertheless, package discontinuities and p/n skew must be minimized as described further above. Furthermore, host ICs should implement EQ capabilities well-beyond minimum Gen5 expectations.
2. **Motherboard Design.** Regardless of dielectric material chosen, we have shown Gen5 PCB routes to have considerable IL at 16 GHz. As such, routes should be kept as short as possible. With cables trending 10x less IL per unit length than PCB routes, it can be wise to offer short routes to cable connections when possible – particularly when the goal is to provide generic connectivity to unknown devices and/or reach.
3. **Add-in Cards.** Given the discontinuities seen in current Gen5 AIC connectors, it can be wise to implement both a min/max IL on an AIC. Adding at least 2 dB IL in the passive interconnect between the active device and edge-finger has been shown to be helpful to

damp connector reflections, assuming this addition does not exacerbate maximum IL requirements.

4. **Cables.** Using cables to achieve interconnect length and flexibility is an excellent option for Gen5 implementation. Obviously, cables come in a huge array of lengths and styles. We believe cables deployed for Gen5 should exhibit IL at or near 0.15 dB/inch, and that this is achievable for a sufficient variety of cabling options. Users of cables should work with cable vendors to verify and qualify this range of IL.
5. **Retimers.** With IL easily reaching 36 dB for many common connection scenarios, no doubt retimers will find use in a variety of Gen5 applications. Nevertheless, because retimers introduce an additional layer of design considerations and complexity, we believe they should be used sparingly – and only after IL budgets and options have been examined and exhausted.

4.4 Lessons from Hardware Bringup

The author's view is that the information shared to this point does not represent merely a classical simulation/measurement exercise, but rather a description of what we learned, practiced, and believe is necessary to get to the bench and power up physical hardware. Our work has proactively mitigated many SI problems and hence we are pleased to report that the majority of our Gen5 links have proven to be functional in hardware with minimal effort. Indeed, given the scale and complexity of most (and certainly our) system designs, discovering issues post-hardware is a serious problem that should be avoided at all (most) costs.

Nevertheless, as of this writing, a variety of problems and challenges remain. Oddly, many items we thought would be difficult turned out to be easy, while things we thought would be easy have turned out to be hard. Specifically,

- Third-party Gen5 Add-in Cards (AICs) have worked better than expected. Good news.
- Host (upstream) connection is more challenging than expected. Problems relate to BIOS changes, excessive IL (particularly when connecting two "root" devices, as in a CPU to an expander/switch), the need/challenge of deploying Retimers to mitigate this IL, and the newness of adding CXL requirements on top of PCIe.
- Deploying Retimers is challenging. Not only must they be placed in the correct location for IL trading and mitigation, they also must correctly implement the entire LTSSM (Link Training and Status State Machine) and even a new low-latency mode for CXL. Bifurcation and clocking present additional issues.
- Shutting off Tx EQ as described in [1] can be helpful yet accessing control of the same can be challenging.
- Protocol Analyzers generally don't help with Signal Integrity signal quantification or issues. PCIe protocol is complex requiring over 100,000 packets to get to state L0 and analyzers do a good job of capturing and abstracting that process. Nevertheless, as a link ratchets up from Gen1 x1 to Gen5 x16, additional lane-specific information regarding EQ training and/or failure that might be expected to be available is harder to access. For now, plan to solve your SI (including EQ) elsewhere and as described herein.

- Eyescan (e.g., eye diagrams captured internal to ICs) unfortunately does not always track with link performance. As such, discuss with IP and component vendors what SI metrics are available, how to properly collect this information, what it means, and how to use the same to debug link problems. Oddly enough, placing even a lower-bandwidth oscilloscope on signals can be quite revealing, once you understand what you're looking at.
- It is preferable to do an FPGA version for a new protocol like CXL prior to a dedicated IC implementation, and this is standard practice.

As we've endeavored to explain and reveal, Gen5 has brought a myriad of SI-related surprises and frustrations. Nevertheless, a key learning for our team is "do your SI homework up-front, triple check it, and if links are failing in hardware, then look elsewhere for the root cause." Indeed, thankfully SI is not "black magic" [1, section 1.1.3] and can significantly be resolved pre-hardware. As such, again assuming up-front SI due diligence as described herein, bringup time can be saved by resisting the inclination to first suspect link failures are due to SI and piling up investigations for the same.

5 Summary and Conclusions

This paper has spent considerable time explaining how and why Gen5's fundamental frequency has significantly changed what had been a "typical" PCI Express experience with insertion loss (IL) in previous generations – primarily due to the IL performance of Gen5 packages, PCBs, and cables. If the reader's PCIe design paradigm is Gen3/4, we cannot stress enough the importance of – at a minimum – applying Table 1 to approximate IL *prior to accepting or pursuing any proposed architectural physical connection.* In short, what had been simple and acceptable in previous generations is no longer. Furthermore, we believe the kind of analysis and work (measurement and simulation) described herein is imperative in ways we have not experienced in a while.

Conclusions derived and described throughout the paper include:

1. Managing Gen5 loss and discontinuities is challenging using contemporary fabrication techniques.
2. Loss Budgeting is imperative for Gen5 to qualify a proposed connection prior to implementation.
3. Expect Gen5 PCB trace loss to be ~1.5 dB/inch. This presumes routing only in stripline, very-low-loss dielectrics, 6 mil wide traces, and HVLP2 copper.
4. Cables can deliver 10x less loss than PCB routes, or 0.15 dB/inch, assuming this is verified by both the vendor and measurement.
5. Nearly every feature on a PCB becomes a discontinuity at Gen5, and hence must be impedance-matched using techniques described in section 3.2.
6. Measurement is important both to validate Gen5 loss and discontinuities and isolate unexpected behaviors. In our case, one of these was an incorrect footprint revealed by a measured impedance.
7. At the system-level, both min and max IL paths should be analyzed.

8. Equalization provided by components is often more powerful than the minimum EQ assumed by the PCIe spec, and this should be quantified.
9. Hardware bringup is simplified by up-front SI work, yet still presents the documented challenges.

It is the authors' hope that the information shared here enables design success for the many Gen5 implementations that will follow.

Acknowledgments

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