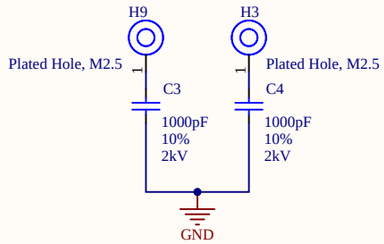
REV.	DESCRIPTION	DATE	APPROVED
A-1	First revision	2021-10-07	J Johnson

MOUNTING HOLES



FIDUCIALS

STANDOFFS

S1

Standoff, Hex, 10mm, M2.5

S2

Standoff, Hex, 10mm, M2.5

S3

Standoff, Hex, 10mm, M2.5

S4

Standoff, Hex, 10mm, M2.5

SCREWS

S5

Machine Screw, M2.5 thread, 4mm length

S6

Machine Screw, M2.5 thread, 4mm length

S7

Machine Screw, M2.5 thread, 4mm length

S11

Machine Screw, M2.5 thread, 4mm length

M.2 MODULE FIXING PARTS

SO1

Standoff, Round, Nylon, 1.6mm

S9

Machine Screw, M2.5 thread, 3mm length
388-238

SO2

Standoff, Round, Nylon, 1.6mm

S8

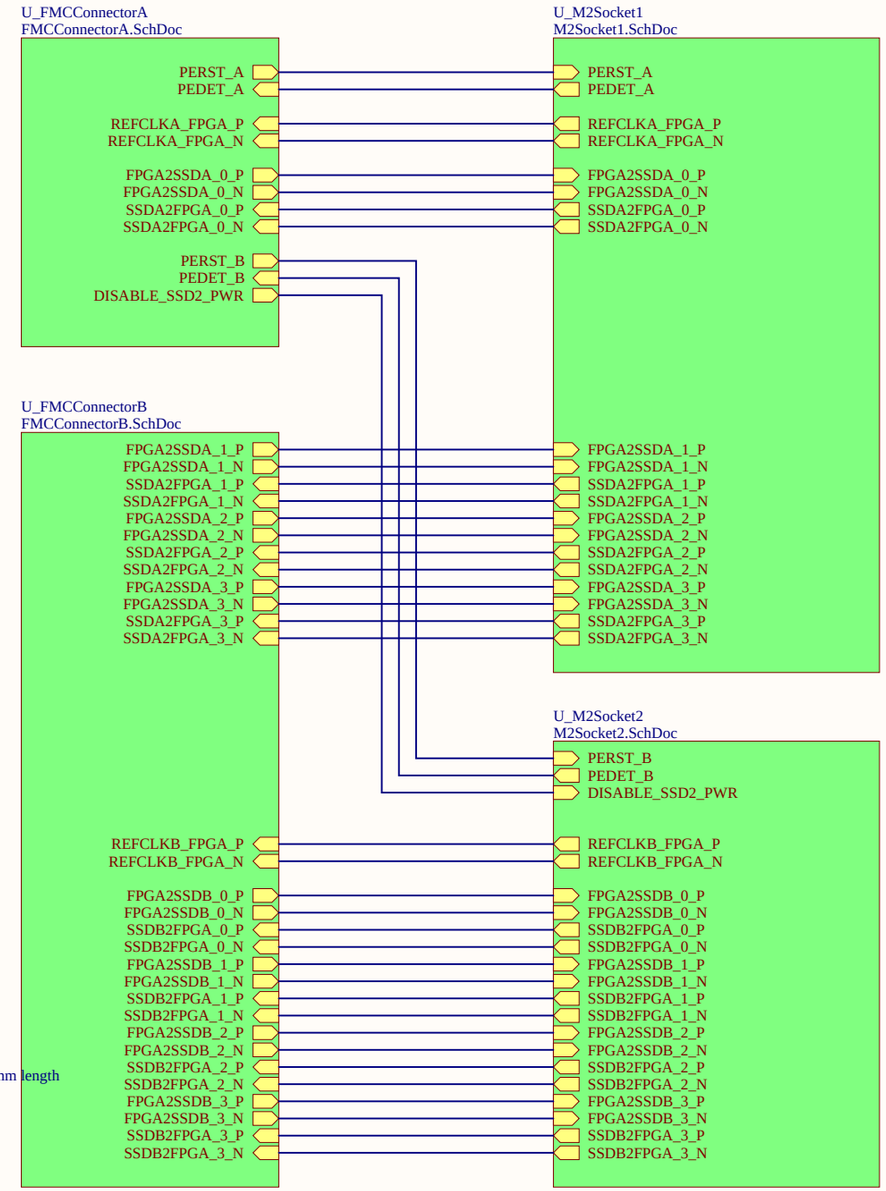
Machine Screw, M2.5 thread, 3mm length
388-238

SO6

Standoff, Round, 2.5mm, M2.5

SO3

Standoff, Round, 2.5mm, M2.5



TITLE	FPGA Drive FMC Gen4		
SHEET	Top		
CONFIG.	Standard		
PROJECT	FPGA Drive FMC Gen4	DRAWN J Johnson	DATE 2021-10-07
SIZE B	SCH P/N. OP063-01-SCH.	REV. A-1	SHEET OF 1 5

REV.	DESCRIPTION	DATE	APPROVED
A-1	First revision	2021-10-07	J Johnson

Routing note:
PCIe data P/N traces must be matched to 5mils

Routing note:
PCIe data pairs must be length matched to 1000mils

Routing note:
Spacing between PCIe data pairs must > 40mils

Sleep mode clock feature not supported. SUSCLK (32kHz clock input) is not connected at the host.

Reference clock parking not supported. CLKREQ# (open drain output driven by M2 module) is not connected at the host.

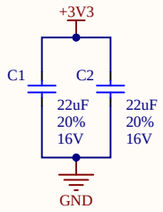
WAKE feature not supported. WAKE# (open drain output driven by M2 module) is not connected at the host.

DEVSLP Sleep mode not supported. DEVSLP input is tied to ground at the host.

M.2 Socket 1 is powered by the FMC connector's 3.3V supply.

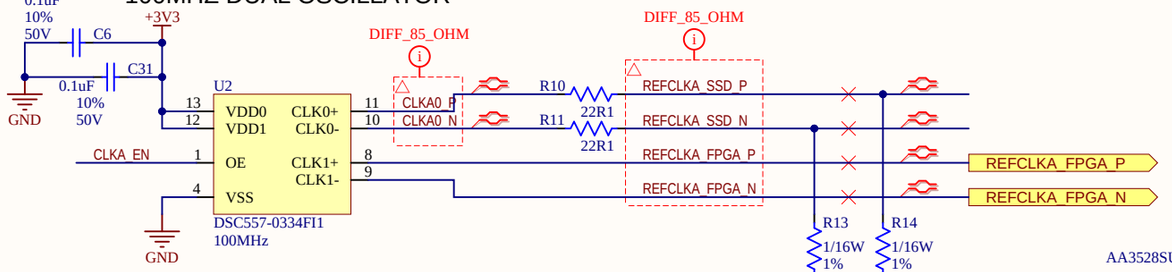
According to VITA 57.1 standard, the 3.3VDC rail must have provision to supply at least 3A. According to M.2 standard, M.2 M-key modules are rated for 2.5A max continuous.

DECOUPLING CAPS



OE pin of DSC557 device has an internal 40k pull-up as specified by datasheet.

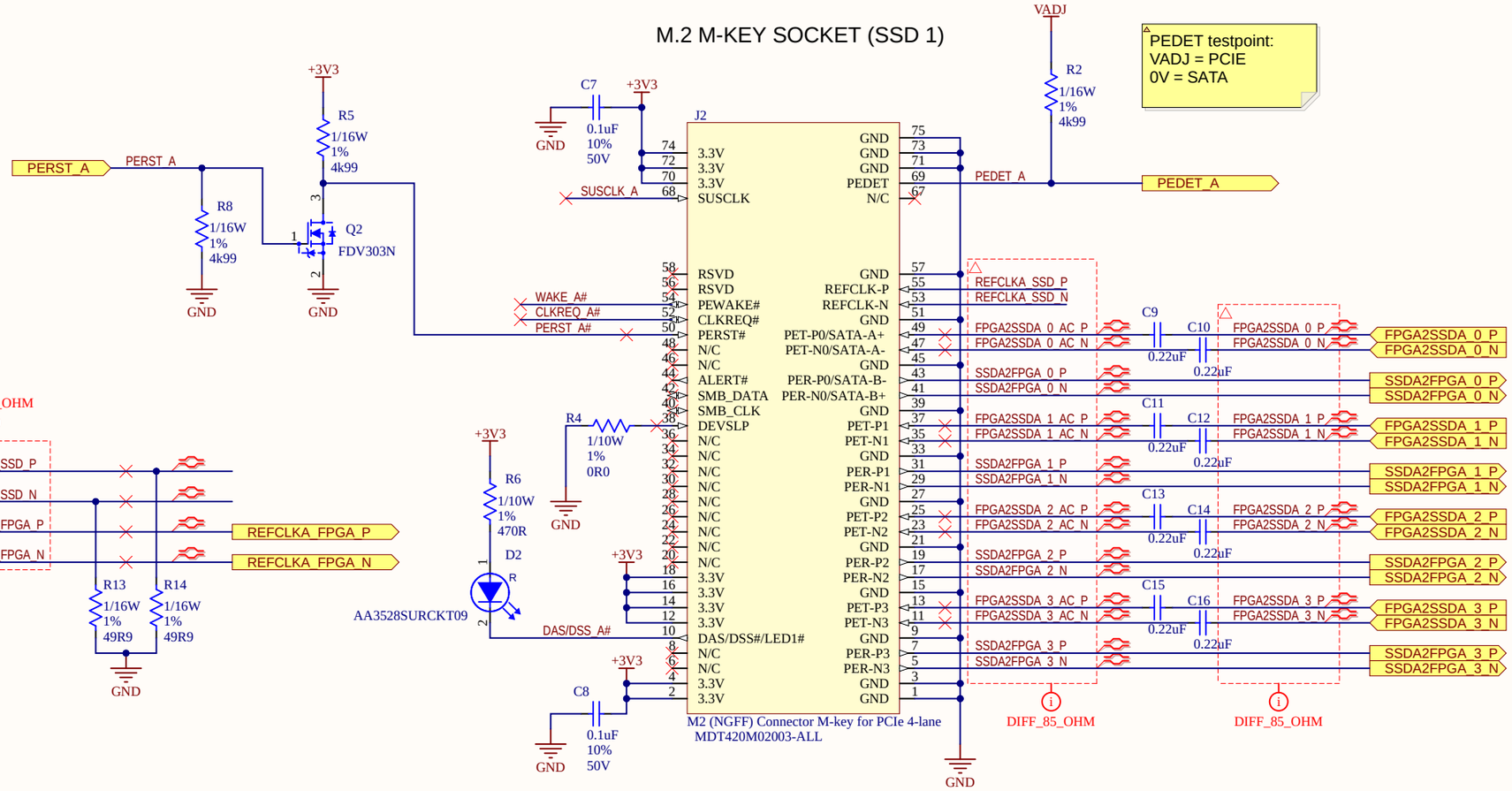
100MHZ DUAL OSCILLATOR



REFCLK_FPGA_P/N PCIe reference clock connects to GBTCLK of the FMC, thus it is required to be LVDS according to Rule 5.54: The reference clocks, GBTCLK, shall use the LVDS signaling standard

M.2 M-KEY SOCKET (SSD 1)

PEDET testpoint:
VADJ = PCIE
0V = SATA



TITLE	FPGA Drive FMC Gen4		
SHEET	M.2 Socket 1		
CONFIG.	Standard		
PROJECT	FPGA Drive FMC Gen4	DRAWN J Johnson	DATE 2021-10-07
SIZE B	SCH P/N. OP063-01-SCH.	REV. A-1	SHEET 2 OF 5

REV.	DESCRIPTION	DATE	APPROVED
A-1	First revision	2021-10-07	J Johnson

Routing note:
PCIe data P/N traces must be matched to 5mils

Routing note:
PCIe data pairs must be length matched to 1000mils

Routing note:
Spacing between PCIe data pairs must > 40mils

OE pin of DSC557 device has an internal 40k pull-up as specified by datasheet.

REFCLK_FPGA_P/N PCIe reference clock connects to GBTCLK of the FMC, thus it is required to be LVDS according to Rule 5.54: The reference clocks, GBTCLK, shall use the LVDS signaling standard

Sleep mode clock feature not supported. SUSCLK (32kHz clock input) is not connected at the host.

Reference clock parking not supported. CLKREQ# (open drain output driven by M2 module) is not connected at the host.

WAKE feature not supported. WAKE# (open drain output driven by M2 module) is not connected at the host.

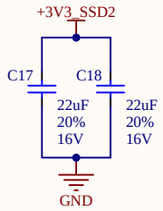
DEVSLP Sleep mode not supported. DEVSLP input is tied to ground at the host.

M.2 Socket 2 is powered by the FMC connector's 12V supply which is converted to 3.3V by DC-DC converter TPS62132RGTR.

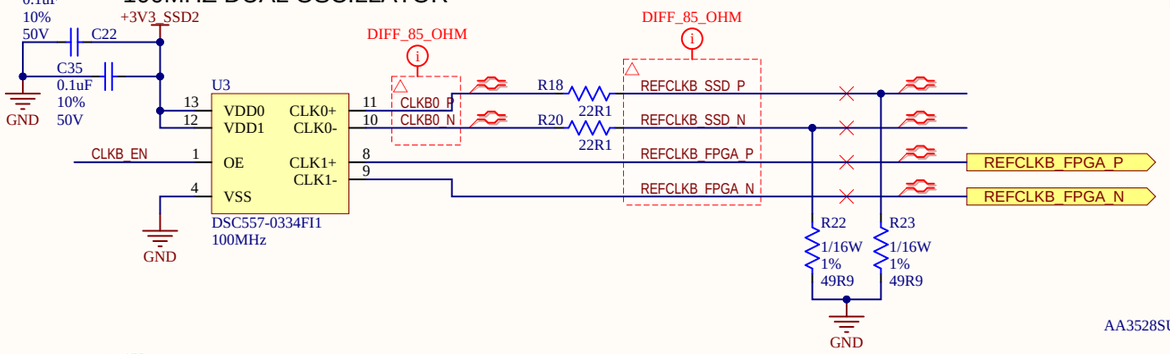
According to M.2 standard, M.2 M-key modules are rated for 2.5A max continuous. According to VITA 57.1 standard, the 12VDC rail must have provision to supply at least 1A. Efficiency of the DC-DC converter is 90% at an output current of 2.5A which equates to a current draw on the 12V rail of less than 0.8A.

PEDET testpoint:
VADJ = PCIE
0V = SATA

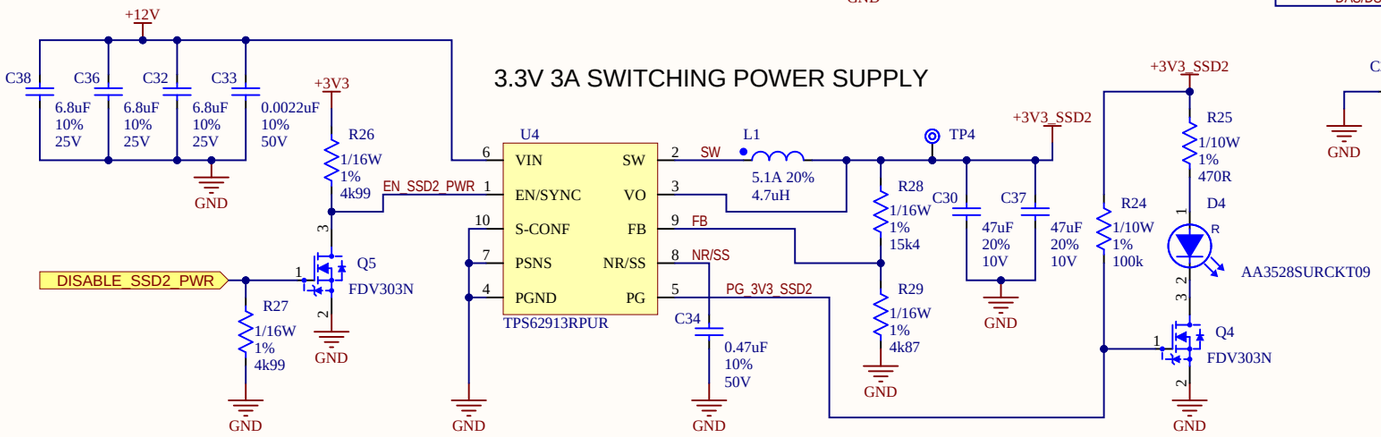
DECOUPLING CAPS

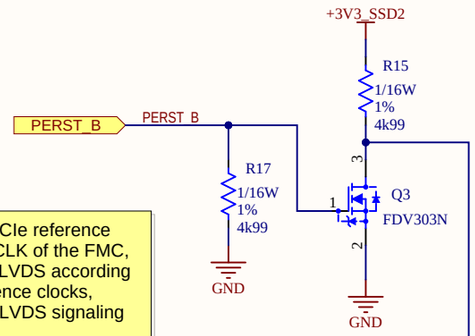


100MHZ DUAL OSCILLATOR

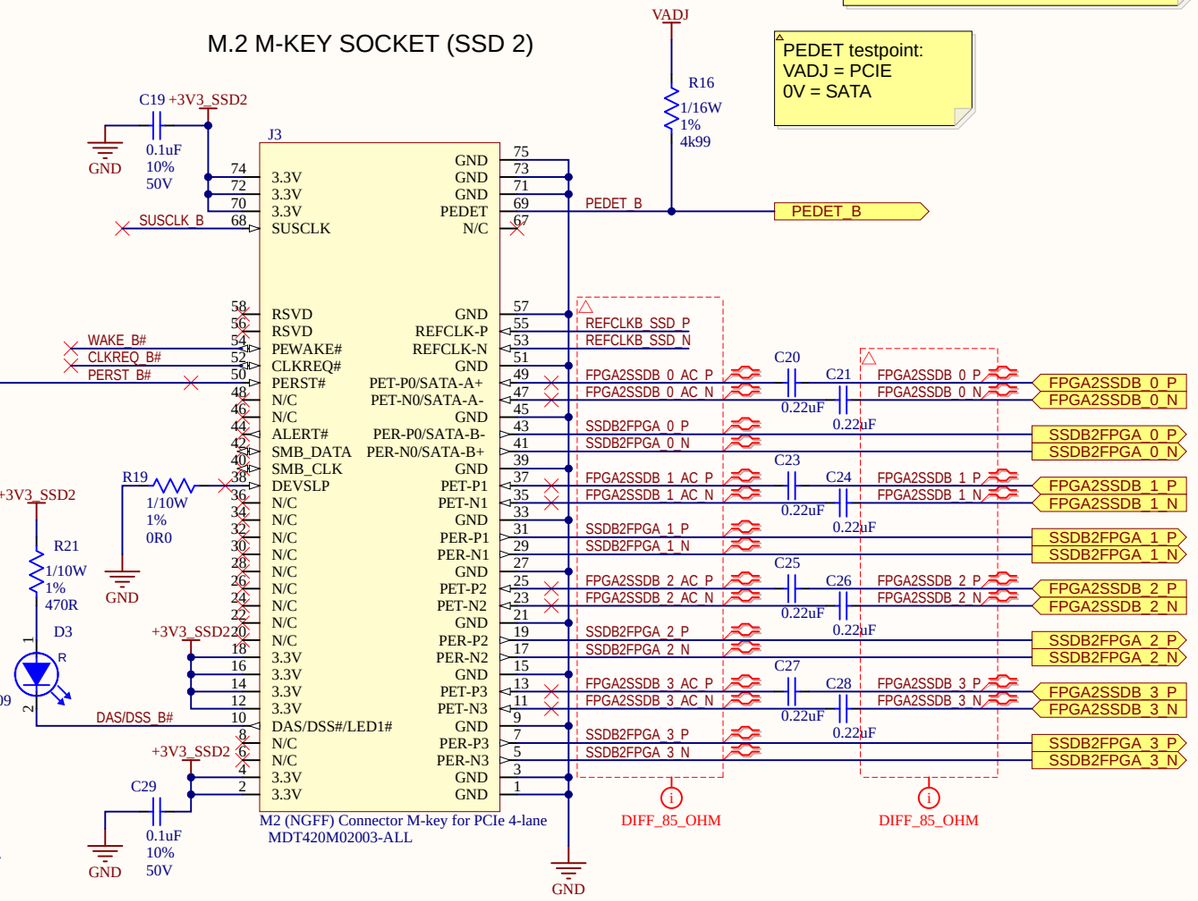


3.3V 3A SWITCHING POWER SUPPLY





M.2 M-KEY SOCKET (SSD 2)



TITLE	FPGA Drive FMC Gen4		
SHEET	M.2 Socket 2		
CONFIG.	Standard		
PROJECT	FPGA Drive FMC Gen4	DRAWN J Johnson	DATE 2021-10-07
SIZE B	SCH P/N. OP063-01-SCH.	REV. A-1	SHEET 3 OF 5

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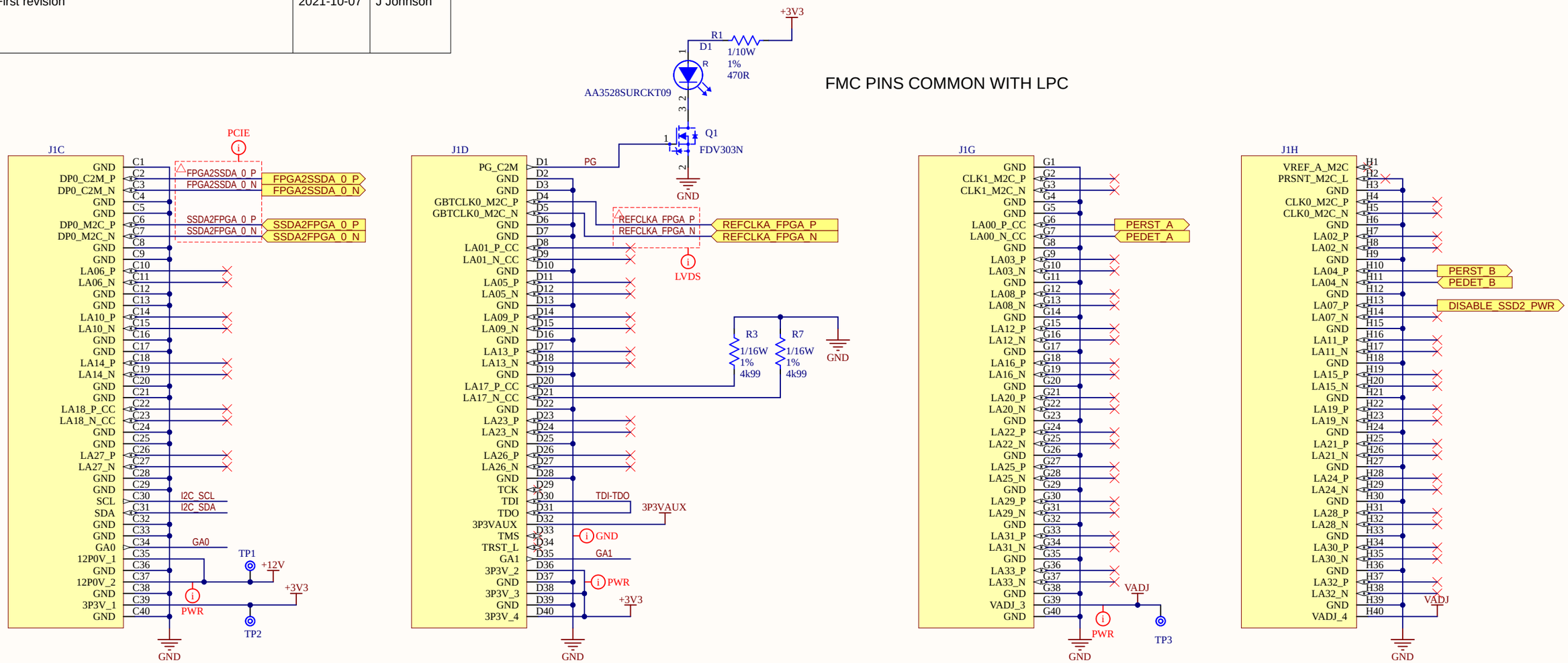
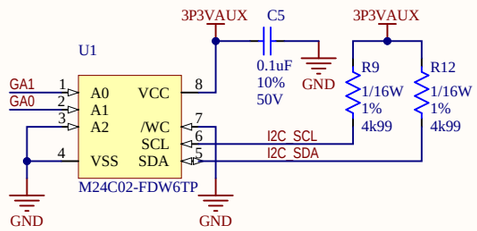
REV.	DESCRIPTION	DATE	APPROVED
A-1	First revision	2021-10-07	J Johnson

FMC PINS COMMON WITH LPC



In accordance with the VITA 57.1 standard: GA0 goes to A1, GA1 goes to A0



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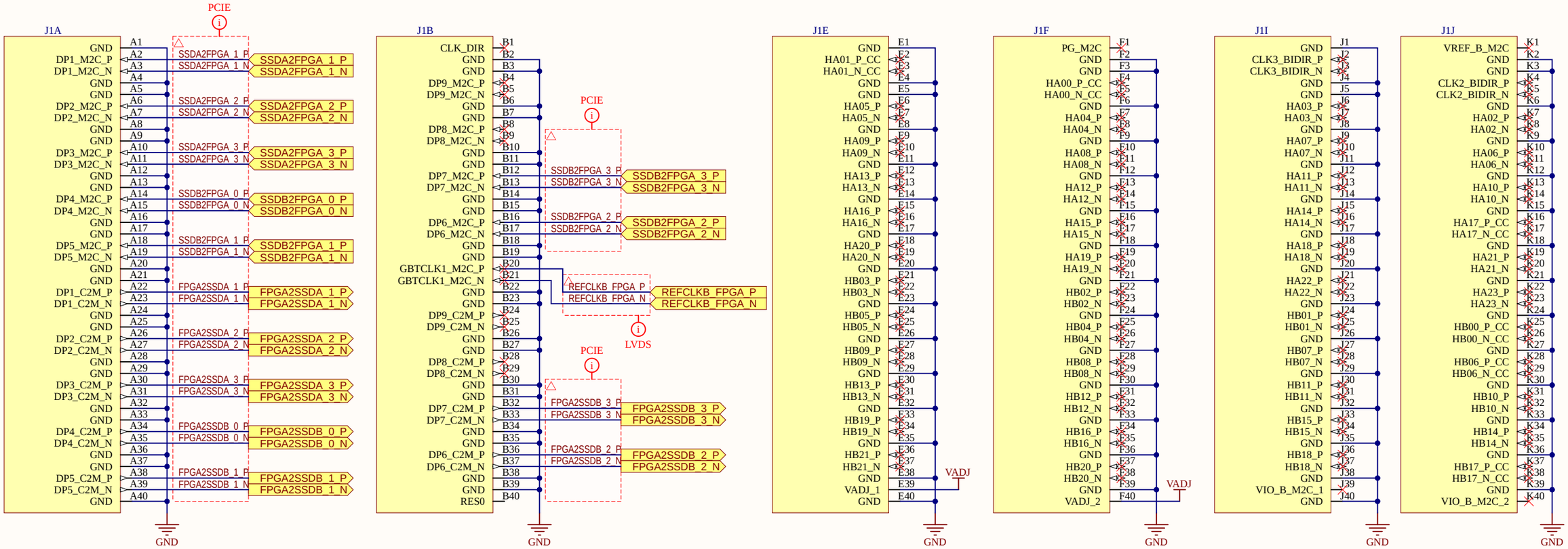
TITLE	FPGA Drive FMC Gen4
SHEET	LPC FMC
CONFIG.	Standard
PROJECT	FPGA Drive FMC Gen4
DRAWN	J Johnson
DATE	2021-10-07
SIZE	B
SCH P/N.	OP063-01-SCH.
REV.	A-1
SHEET OF	4 5

REV.	DESCRIPTION	DATE	APPROVED
A-1	First revision	2021-10-07	J Johnson

HPC FMC PINS



opsero ELECTRONIC DESIGN

TITLE	FPGA Drive FMC Gen4		
SHEET	HPC FMC		
CONFIG.	Standard		
PROJECT	FPGA Drive FMC Gen4	DRAWN J Johnson	DATE 2021-10-07
SIZE B	SCH P/N. OP063-01-SCH.	REV. A-1	SHEET 5 OF 5