REV.	DESCRIPTION	DATE	APPROVED
A-1	First revision	2024-05-01	J Johnson

S1

Standoff, Hex, 10mm, M2.5

S2

Standoff, Hex, 10mm, M2.5

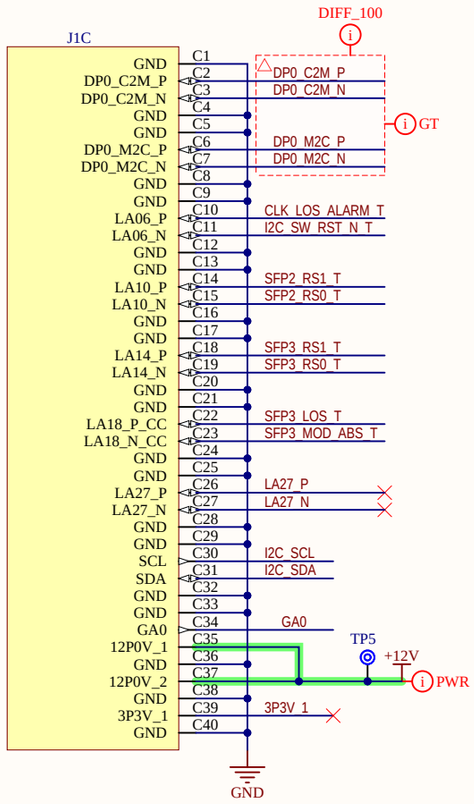
S5

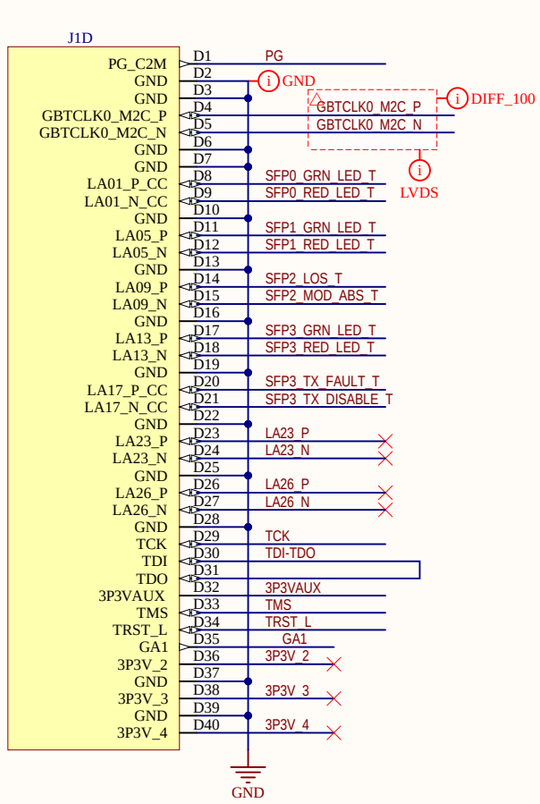
Machine Screw, M2.5 thread, 4mm length

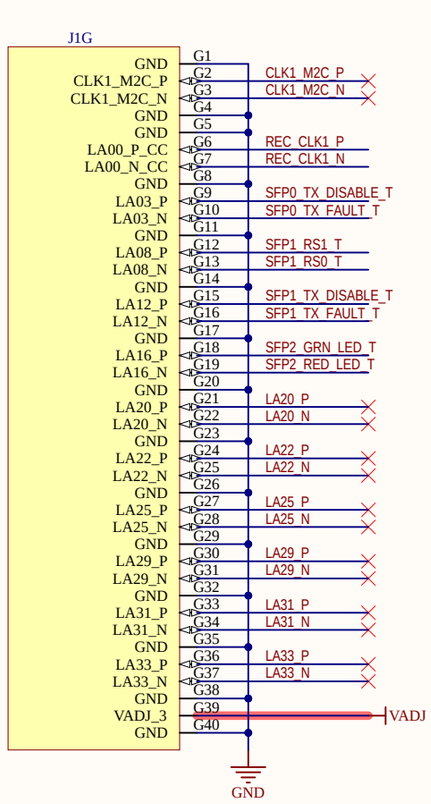
S6

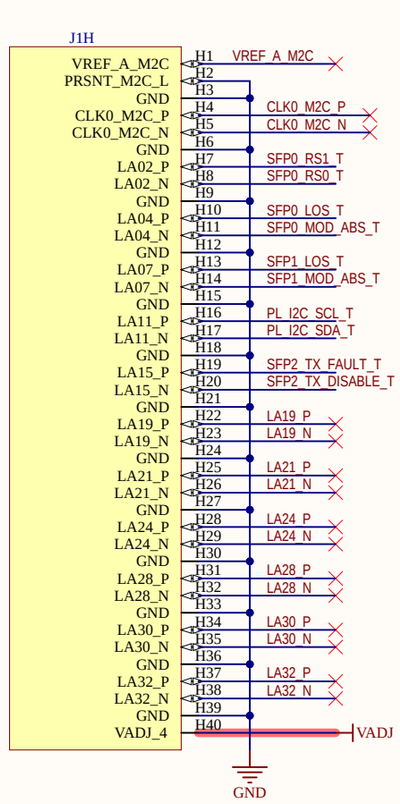
Machine Screw, M2.5 thread, 4mm length

FMC PINS COMMON WITH LPC

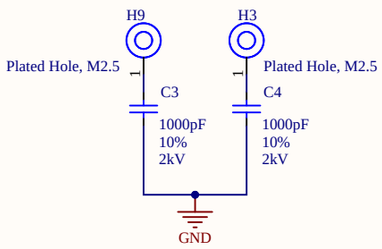






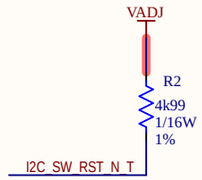


MOUNTING HOLES



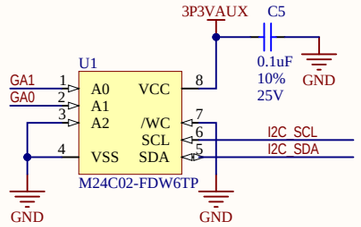
FIDUCIALS

DEFAULTS



I2C Switch reset signal is pulled up in case the user has not connected this pin in the FPGA design.

EEPROM



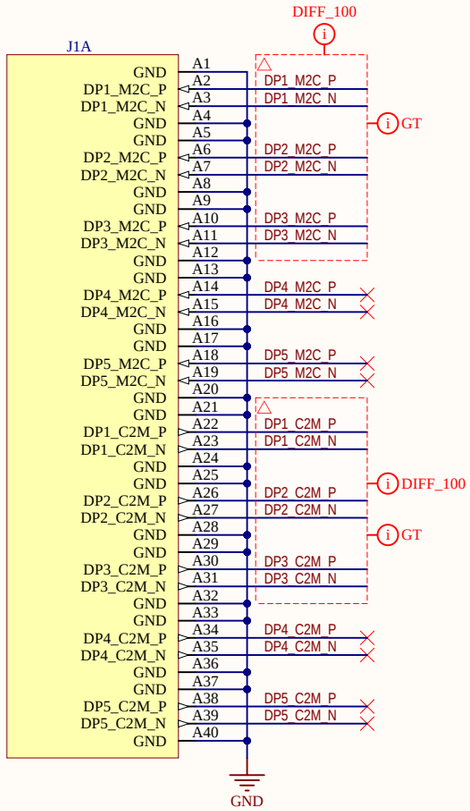
In accordance with the VITA 57.1 standard: GA0 goes to A1, GA1 goes to A0

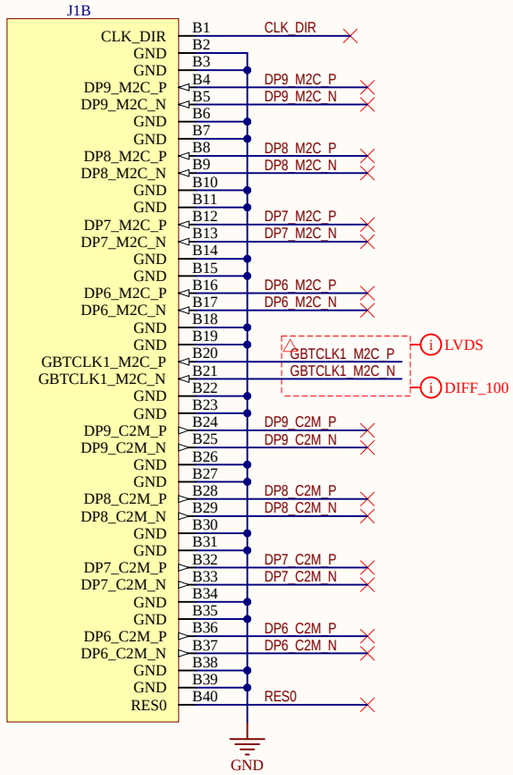
opsero ELECTRONIC DESIGN

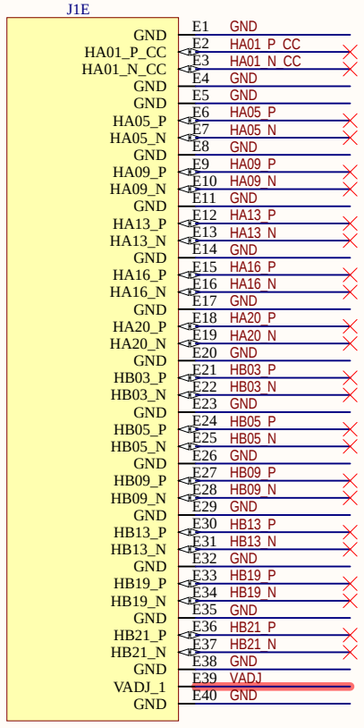
TITLE	Quad SFP28 FMC		
SHEET	LPC FMC		
CONFIG.	Standard		
PROJECT	Ethernet FMC	DRAWN J Johnson	DATE 2024-05-01
SIZE B	SCH P/N. OP081-01-SCH.	REV. A-1	SHEET 1 OF 5

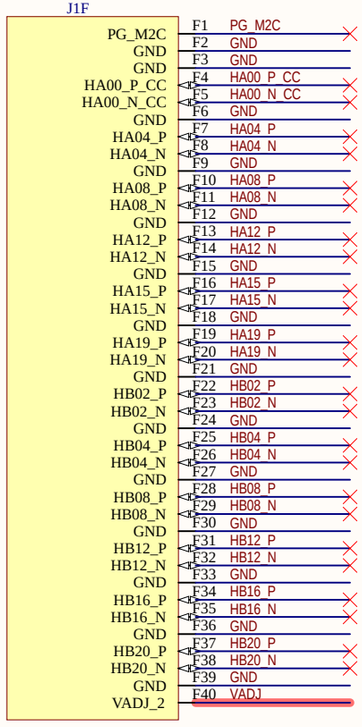
REV.	DESCRIPTION	DATE	APPROVED
A-1	First revision	2024-05-01	J Johnson

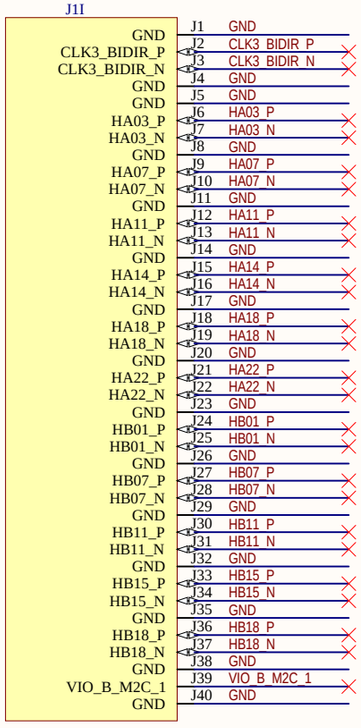
HPC FMC PINS

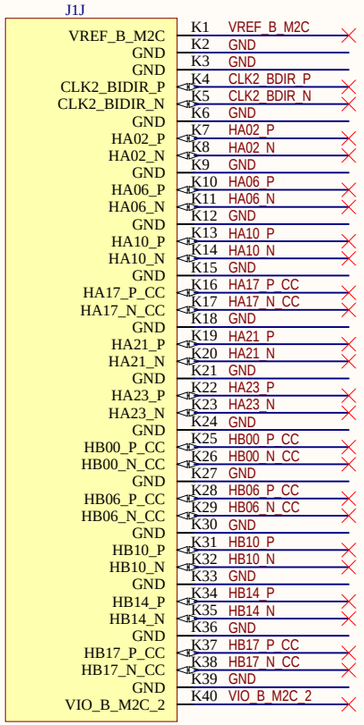












opsero ELECTRONIC DESIGN

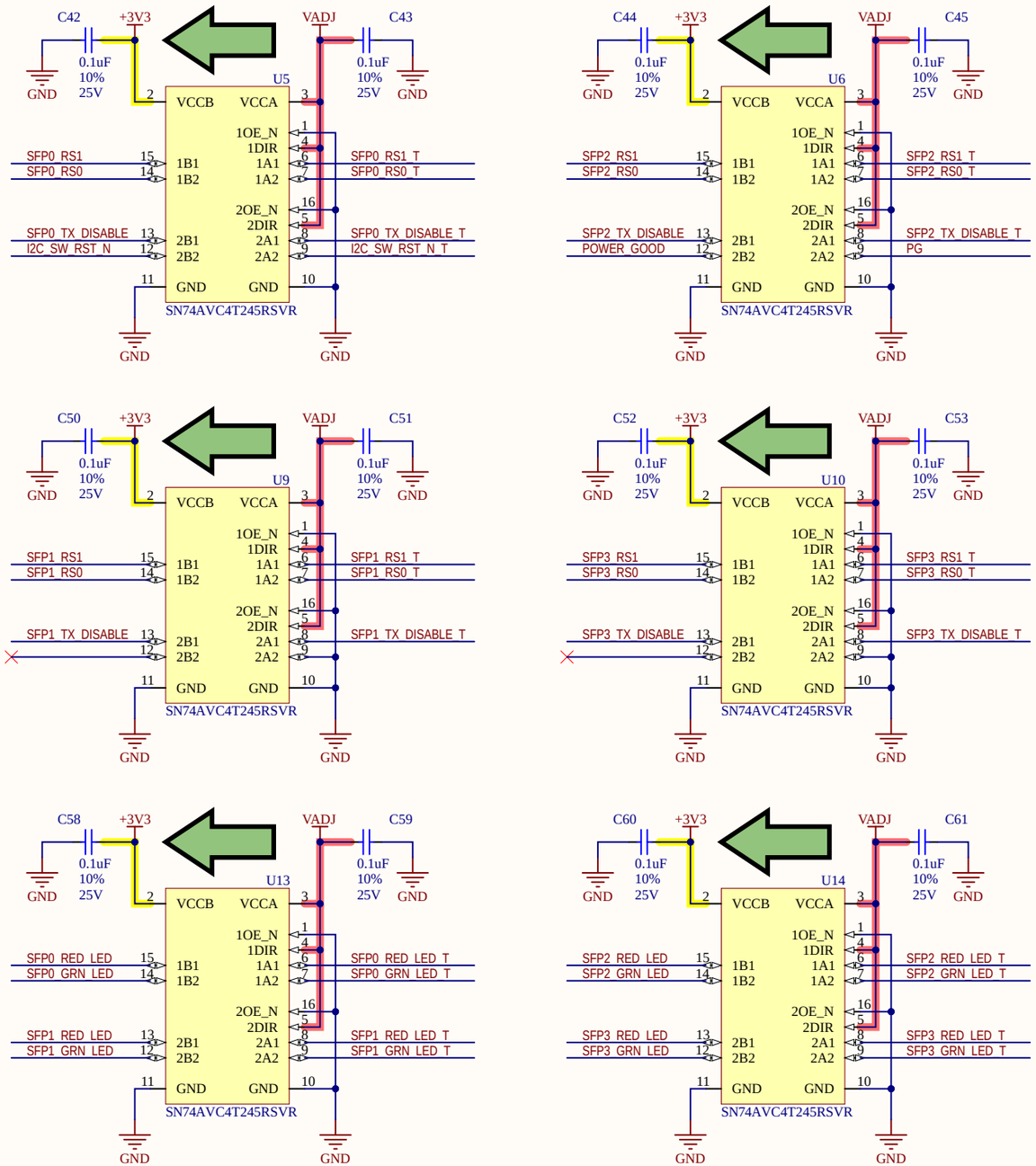
TITLE	Quad SFP28 FMC
SHEET	HPC FMC
CONFIG.	Standard
PROJECT	Ethernet FMC
DRAWN	J Johnson
DATE	2024-05-01
SIZE	B
SCH P/N.	OP081-01-SCH.
REV.	A-1
SHEET	2 OF 5

REV.	DESCRIPTION	DATE	APPROVED
A-1	First revision	2024-05-01	J Johnson

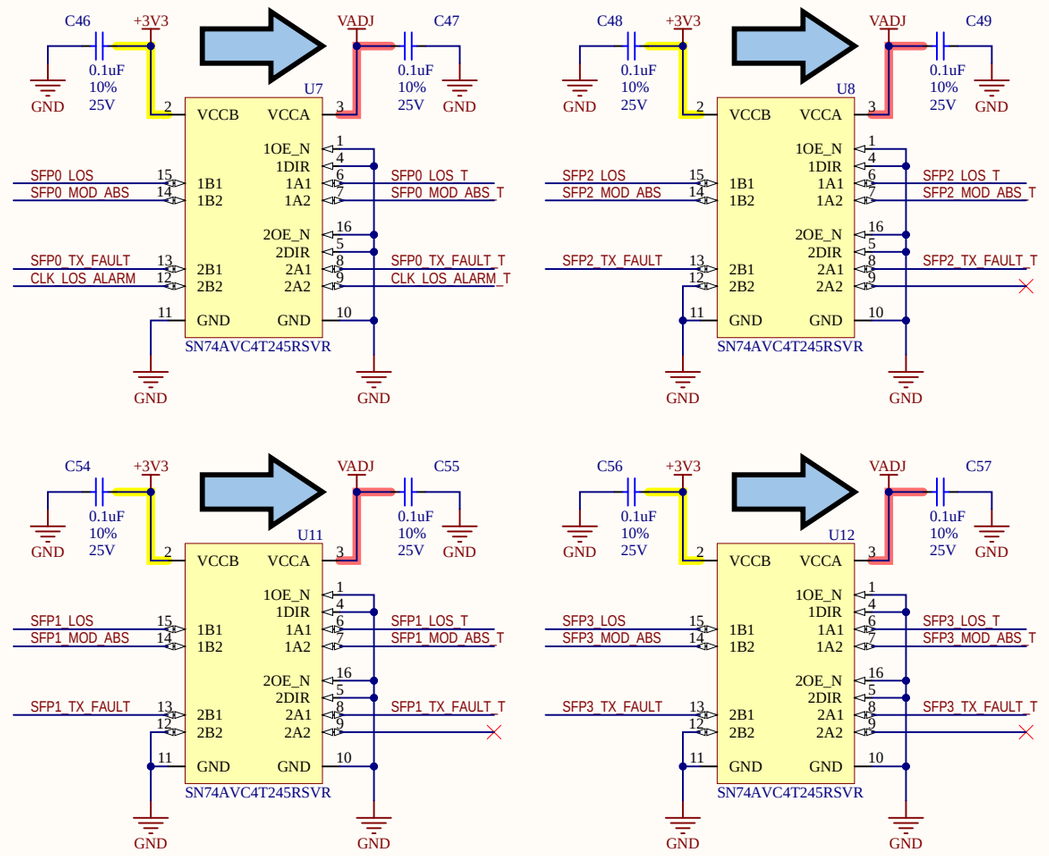
VOLTAGE TRANSLATION

DIR	SIGNAL FLOW
INPUT	
LOW	B -> A
HIGH	A -> B

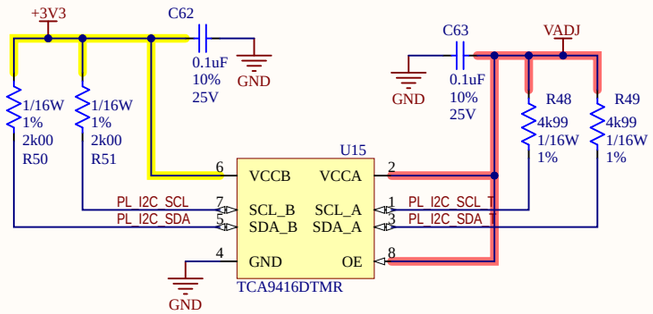
VADJ to 3V3 I/Os



3V3 to VADJ I/Os



I2C VOLTAGE TRANSLATION

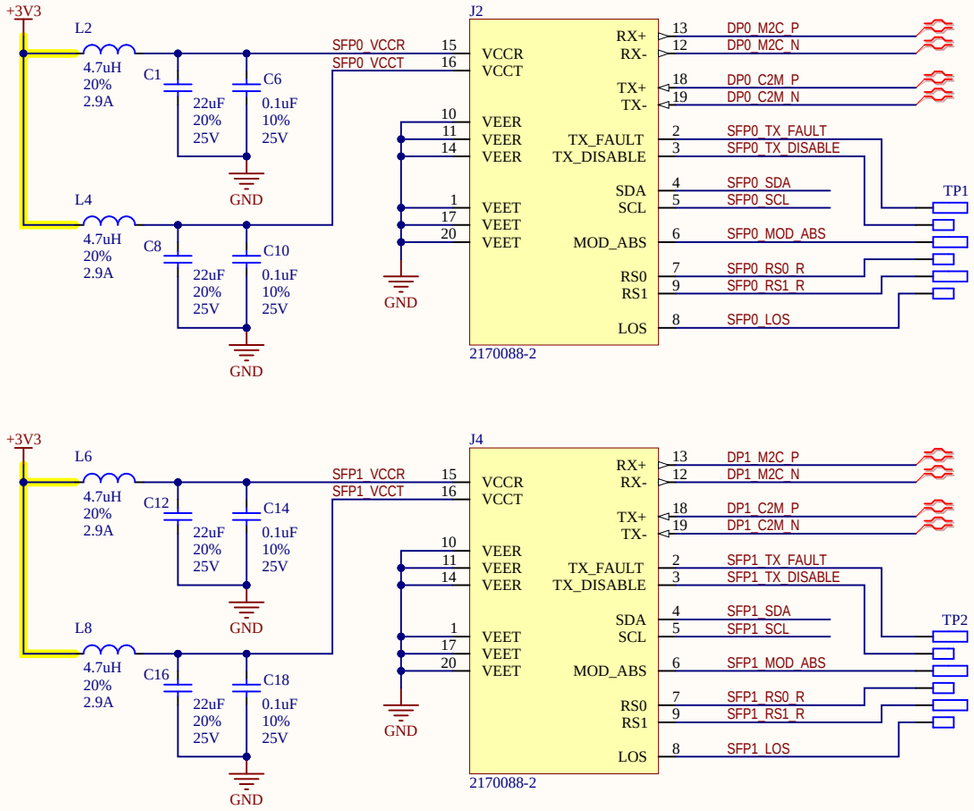


opsero ELECTRONIC DESIGN

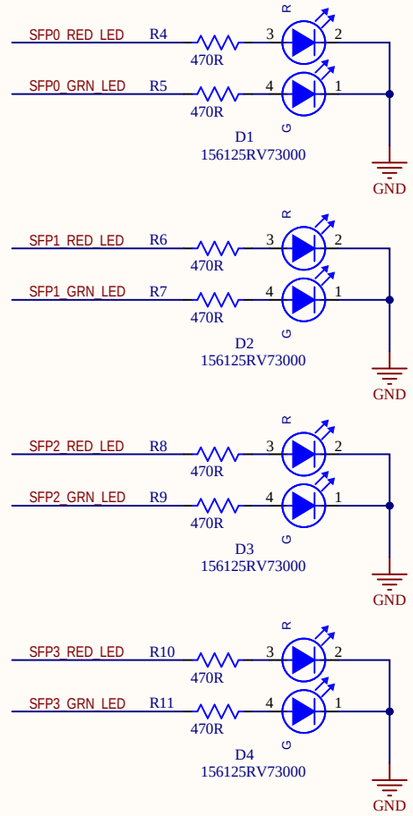
TITLE	Quad SFP28 FMC
SHEET	Voltage Translation
CONFIG.	Standard
PROJECT	Ethernet FMC
DRAWN	J Johnson
DATE	2024-05-01
SIZE	B
SCH P/N.	OP081-01-SCH.
REV.	A-1
SHEET OF	3 5

REV.	DESCRIPTION	DATE	APPROVED
A-1	First revision	2024-05-01	J Johnson

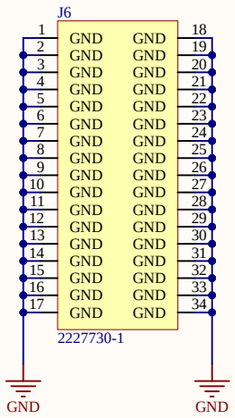
zSFP+ CONNECTORS



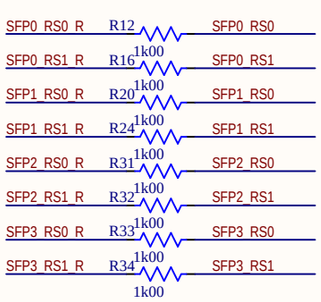
SFP LEDS



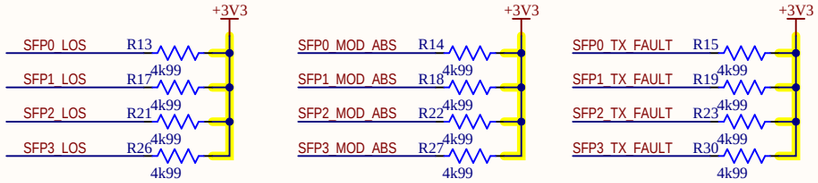
QUAD zSFP+ CAGE



SFP RATE SELECT



SFP OUTPUT PULL-UPS



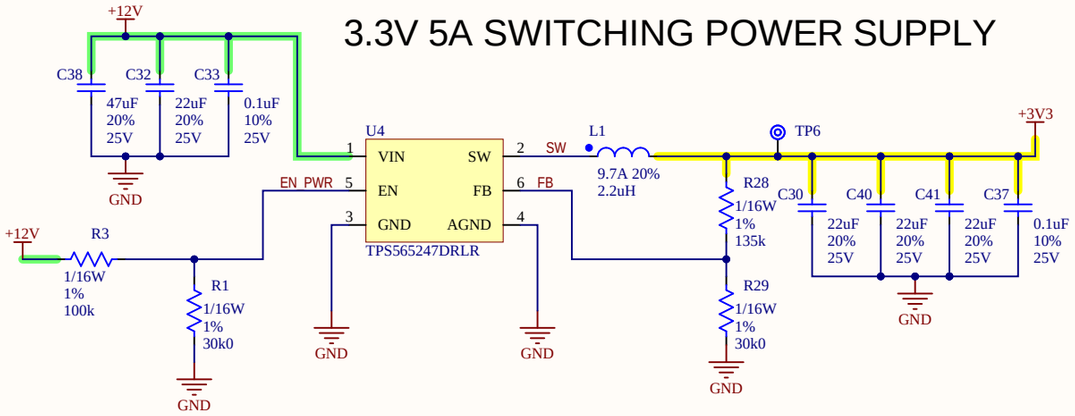
We pull up to 3.3V and then translate to VADJ (rather than just pulling up to VADJ) because some SFP modules specify a minimum pull-up voltage that is greater than 1.5V (ie. greater than the max VADJ of the Versal boards).

opsero ELECTRONIC DESIGN

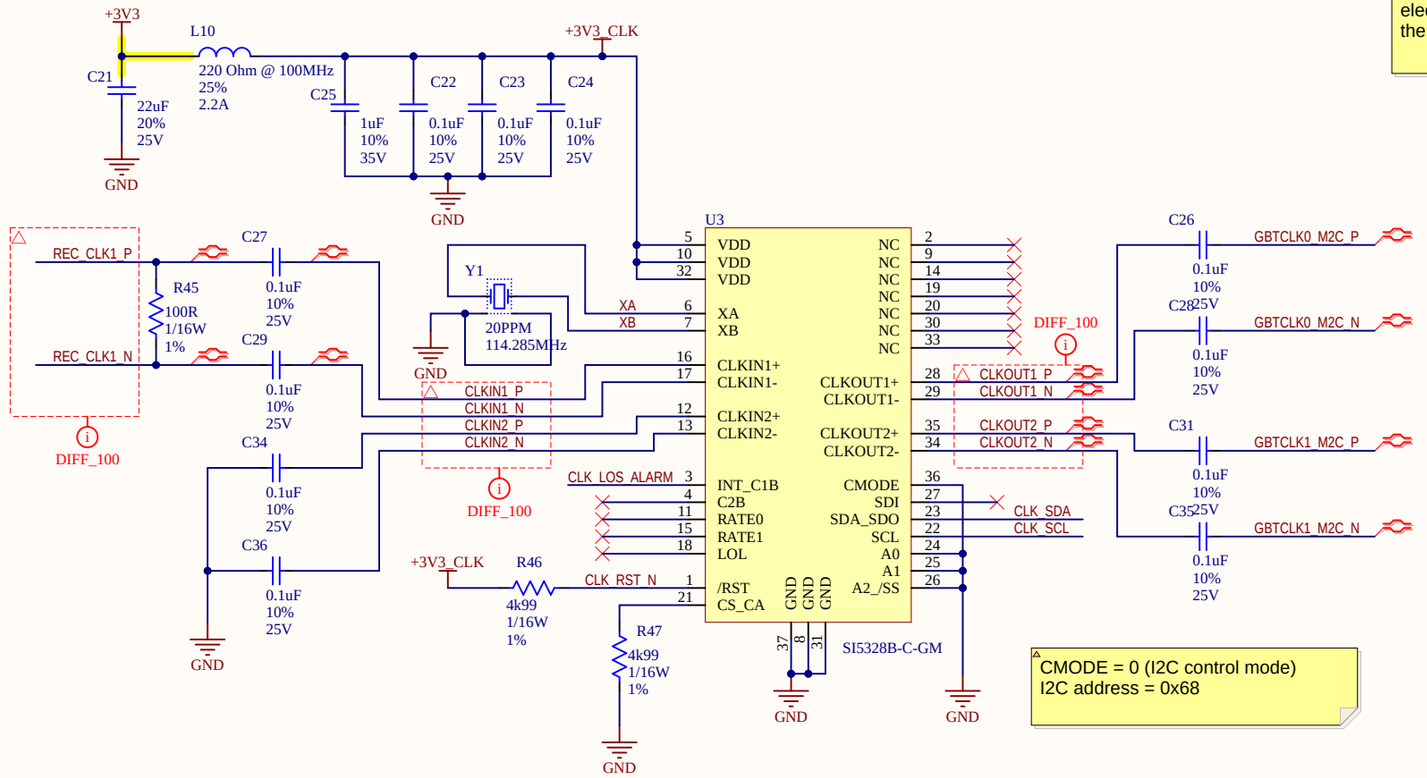
TITLE	Quad SFP28 FMC
SHEET	4x zSFP+ Cage
CONFIG.	Standard
PROJECT	Ethernet FMC
DRAWN	J Johnson
DATE	2024-05-01
SIZE	B
SCH P/N.	OP081-01-SCH.
REV.	A-1
SHEET OF	4 5

REV.	DESCRIPTION	DATE	APPROVED
A-1	First revision	2024-05-01	J Johnson

3.3V 5A SWITCHING POWER SUPPLY



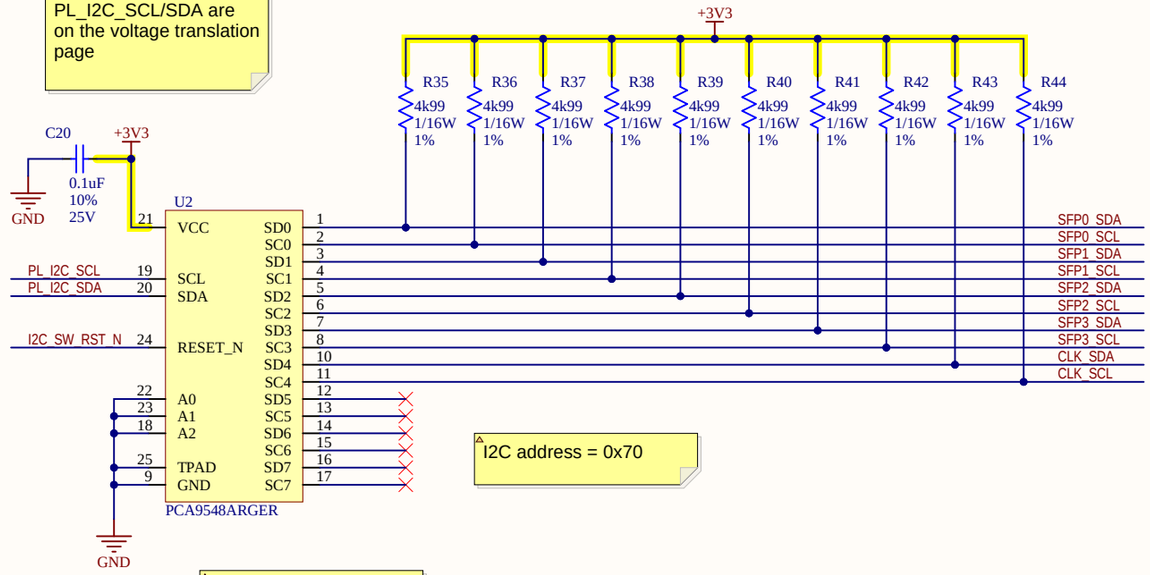
JITTER-ATTENUATING CLOCK MULTIPLIER



CMODE = 0 (I2C control mode)
I2C address = 0x68

I2C SWITCH

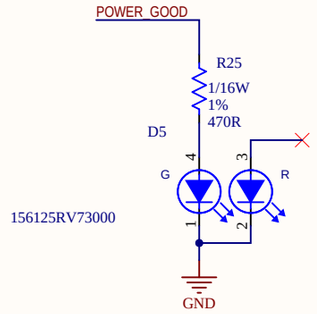
Pull-up resistors for PL_I2C_SCL/SDA are on the voltage translation page



I2C address = 0x70

Thermal pad has no electrical connection in the IC

POWER GOOD LED



For the POWER GOOD LED to turn ON, the FMC's PG signal must be HIGH and the 3.3V from the buck converter must be active. Failure from either of those will result in this LED being OFF.

opsero ELECTRONIC DESIGN

TITLE	Quad SFP28 FMC
SHEET	Power, Clocks and I2C Switch
CONFIG.	Standard
PROJECT	Ethernet FMC
DRAWN	J Johnson
DATE	2024-05-01
SIZE	B
SCH P/N.	OP081-01-SCH.
REV.	A-1
SHEET	5 OF 5