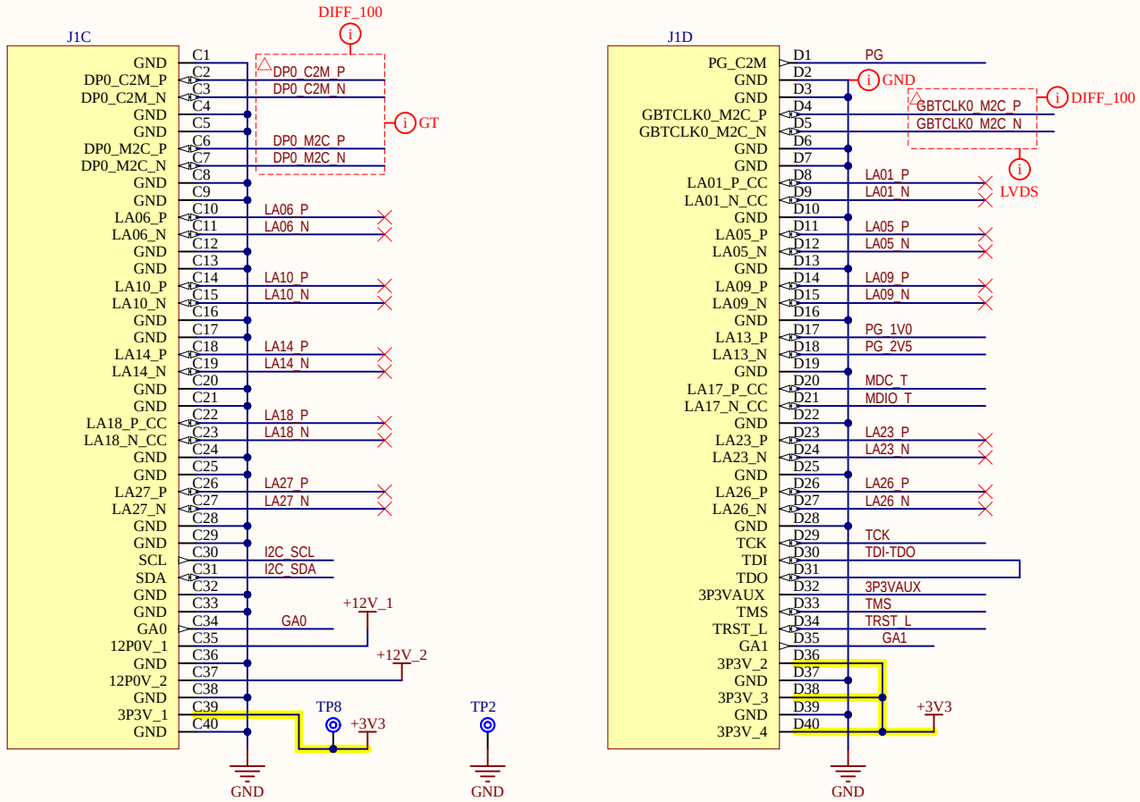
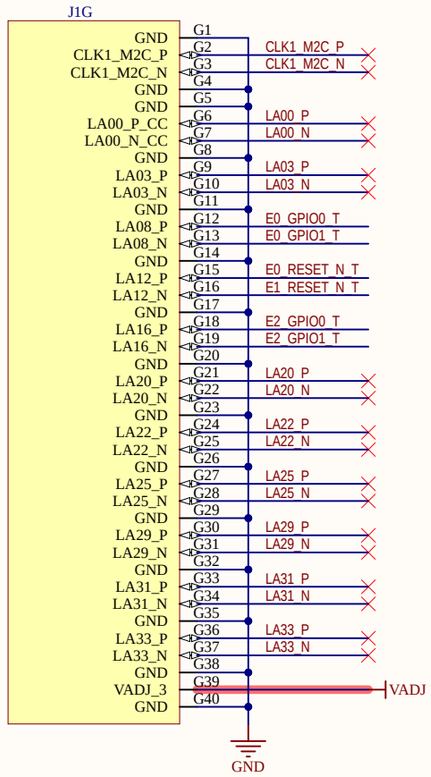
REV.	DESCRIPTION	DATE	APPROVED
A-1	First revision	2024-05-24	J Johnson

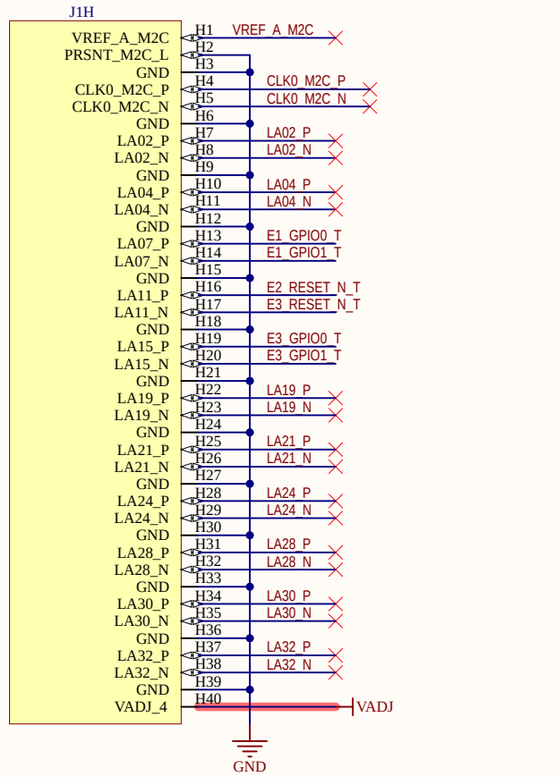
FIDUCIALS

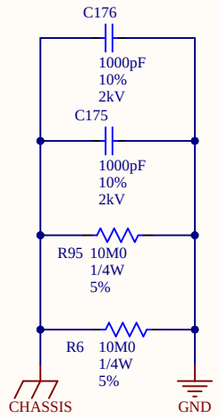
F1 Fiducial F2 Fiducial F3 Fiducial

FMC PINS COMMON WITH LPC

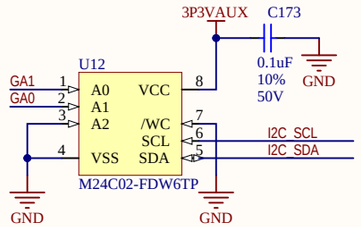






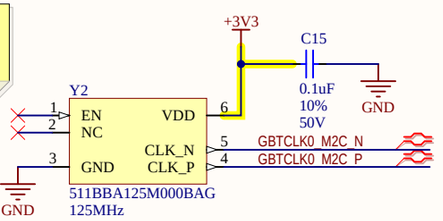


EEPROM



In accordance with the VITA 57.1 standard: GA0 goes to A1, GA1 goes to A0

Si511 has internal pull-up on the enable pin

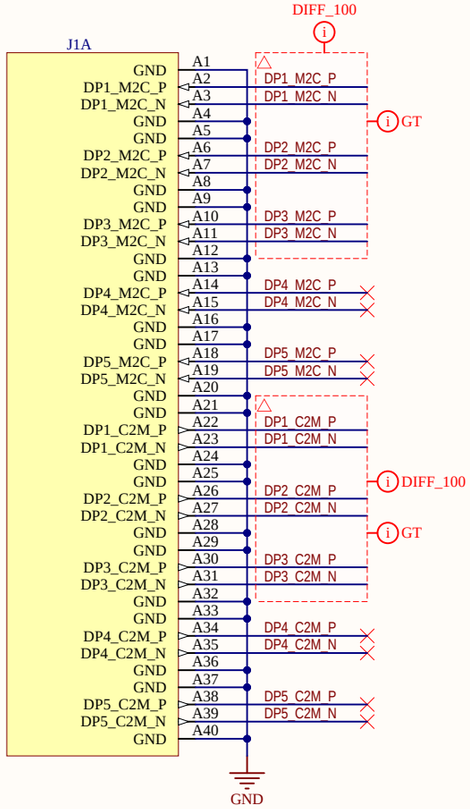


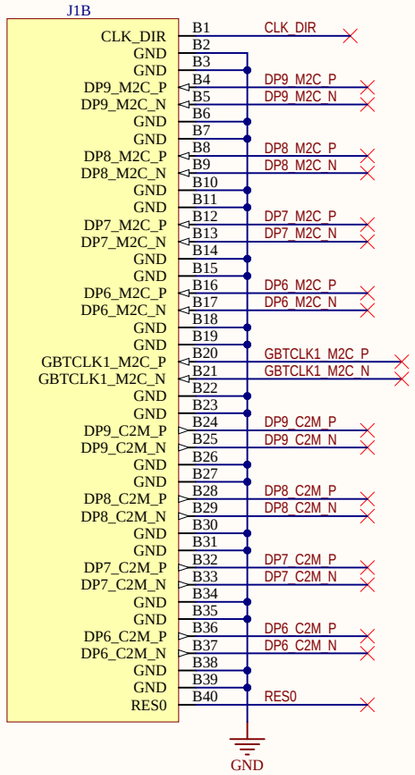
opsero ELECTRONIC DESIGN

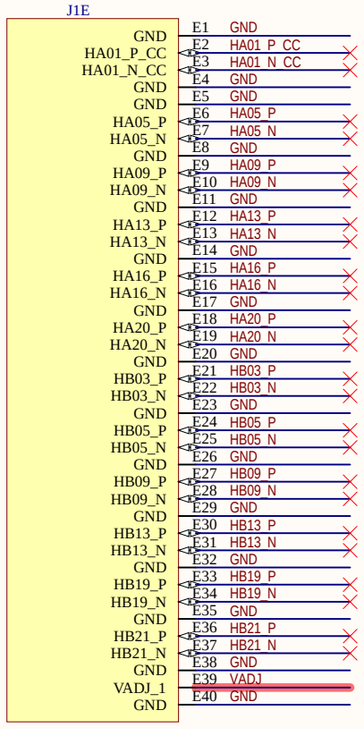
TITLE	Ethernet FMC Max
SHEET	LPC FMC
CONFIG.	Standard
PROJECT	Ethernet FMC
DRAWN	J Johnson
DATE	2024-05-24
SIZE	B
SCH P/N.	OP080-01-SCH.
REV.	A-1
SHEET OF	1 7

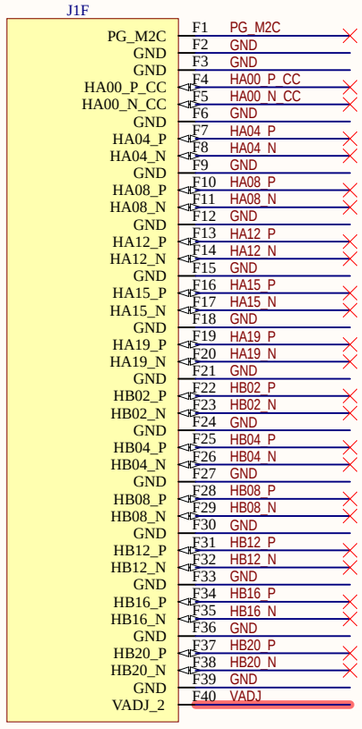
REV.	DESCRIPTION	DATE	APPROVED
A-1	First revision	2024-05-24	J Johnson

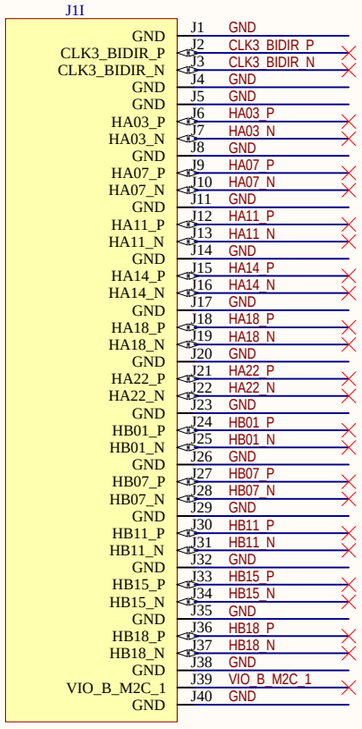
HPC FMC PINS

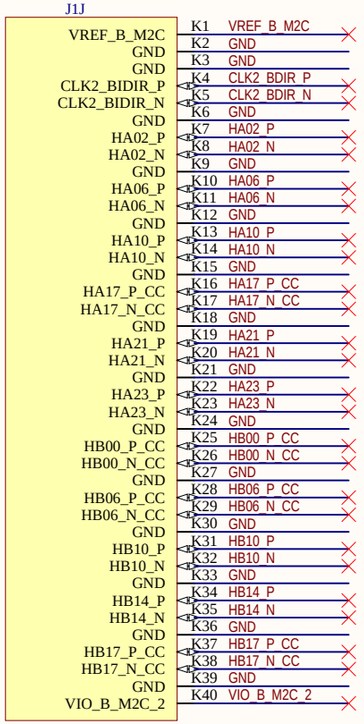












opsero ELECTRONIC DESIGN

TITLE	Ethernet FMC Max
SHEET	HPC FMC
CONFIG.	Standard
PROJECT	Ethernet FMC
DRAWN	J Johnson
DATE	2024-05-24
SIZE	B
SCH P/N.	OP080-01-SCH.
REV.	A-1
SHEET OF	2 7

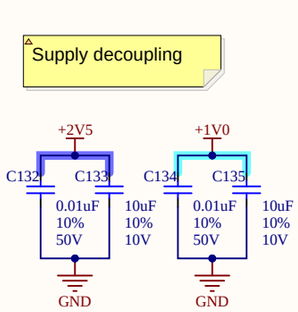
REV.	DESCRIPTION	DATE	APPROVED
A-1	First revision	2024-05-24	J Johnson

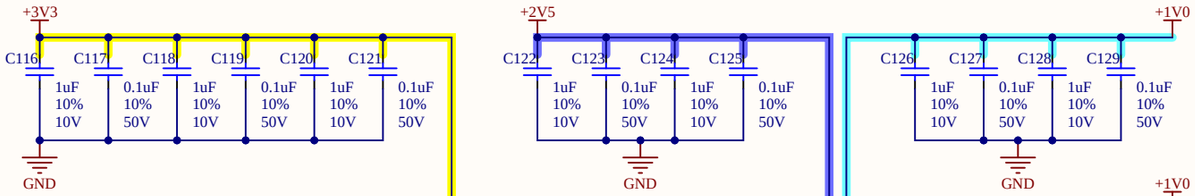
Expected maximum power consumption according to SNLA241:

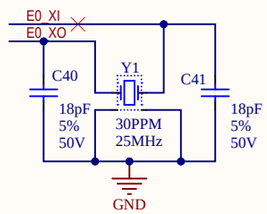
* VDDIO (3.3V): 58.72mA (25 deg, 100% utilisation)
* VDDA2P5 (2.5V): 135.18mA (25 deg, 100% utilisation)
* VDDA1P0 (1V): 124.66mA (105 deg)

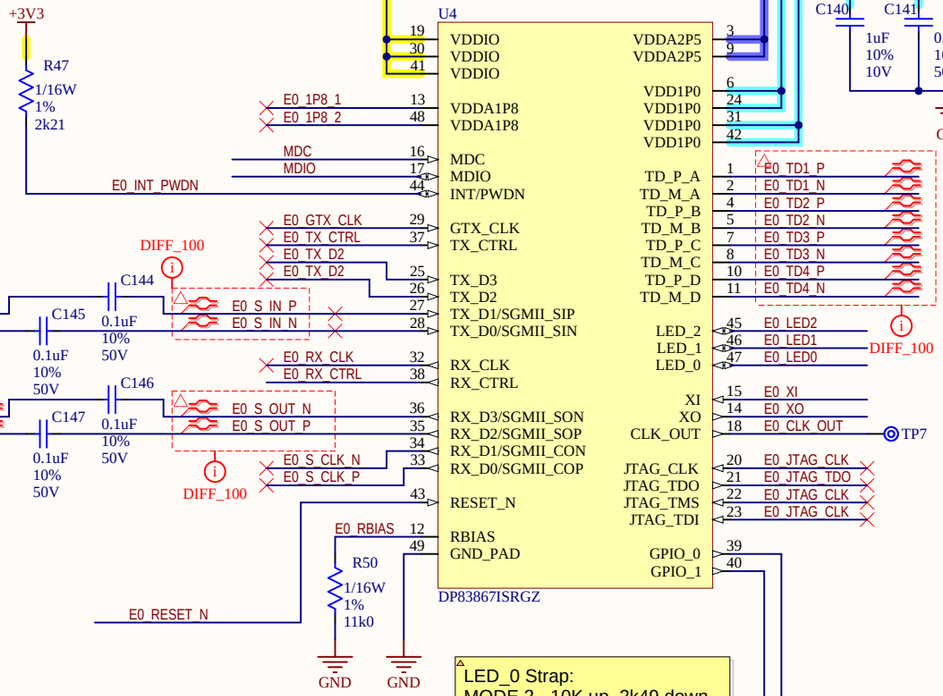
Routing note:
* MDI traces must be 50R to ground and 100R differential impedance
* MDI traces no longer than 2000mils
* MDI traces length matched to 20mils

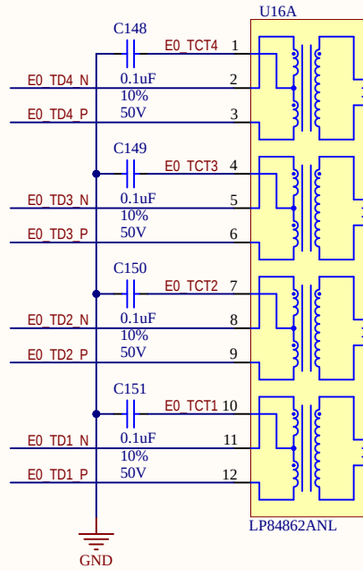
Supply decoupling

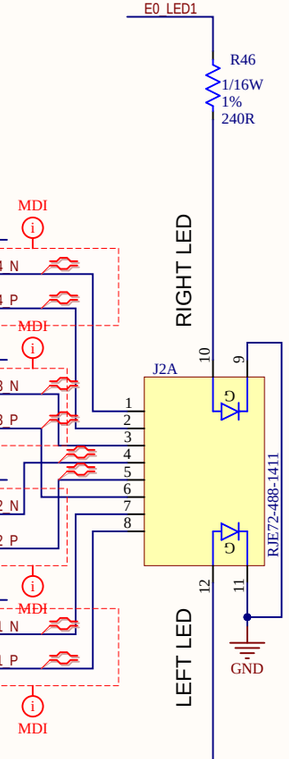






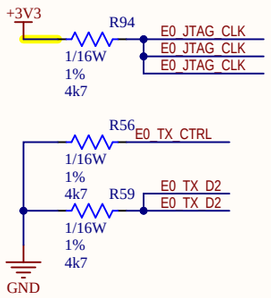




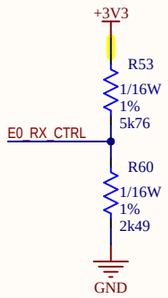


Routing notes:
* SGMII pairs must be routed with 100R differential impedance
* Skew within a pair must be matched to 30mils

Pullups and pulldowns for unused inputs



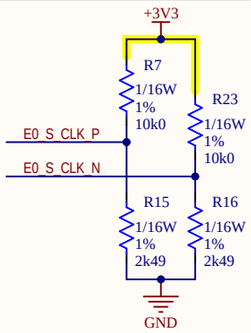
RX_CTRL Strap:
MODE 3 - 5k76 up, 2k49 down
Autoneg disable = 0



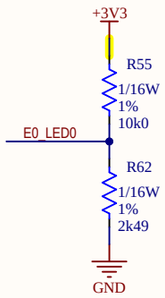
PHY address = 0001

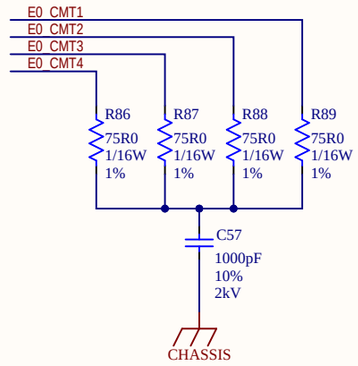
RX_D0 (S_CLK_P) Strap:
MODE 2 - 10k up, 2k49 down
PHY addr [1:0] = 01

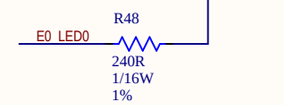
RX_D2 (S_OUT_P) Strap:
MODE 1 - no resistors
PHY addr [3:2] = 00



LED_0 Strap:
MODE 2 - 10K up, 2k49 down
Mirror Enable = 0
SGMII Enable = 1







opsero ELECTRONIC DESIGN

TITLE	Ethernet FMC Max
SHEET	Ethernet PHY 0
CONFIG.	Standard
PROJECT	Ethernet FMC
DRAWN	J Johnson
DATE	2024-05-24
SIZE	B
SCH P/N.	OP080-01-SCH.
REV.	A-1
SHEET OF	3 7

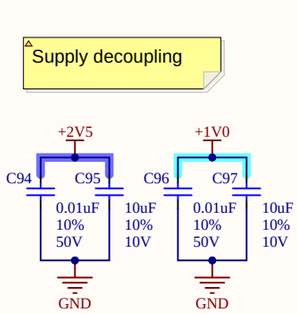
REV.	DESCRIPTION	DATE	APPROVED
A-1	First revision	2024-05-24	J Johnson

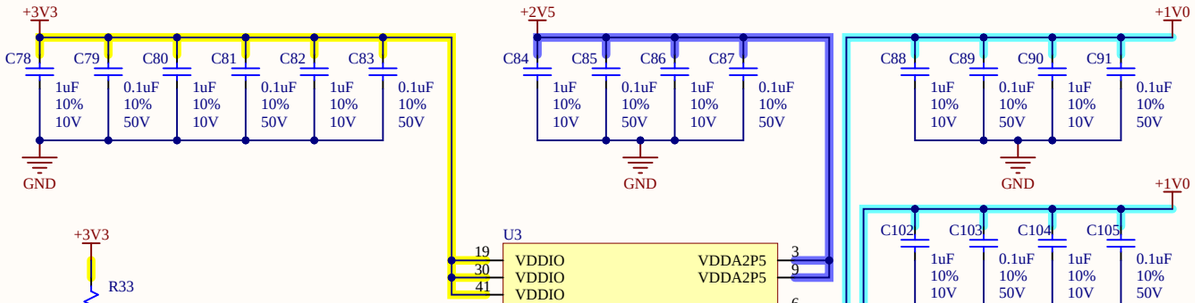
Expected maximum power consumption according to SNLA241:

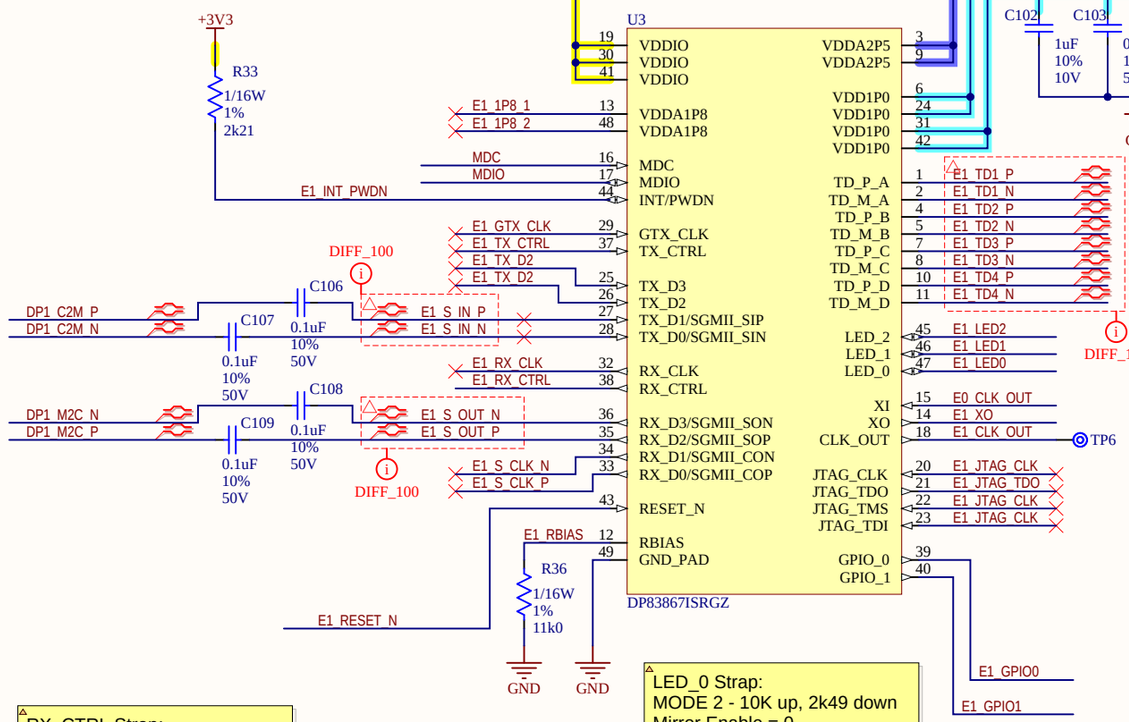
* VDDIO (3.3V): 58.72mA (25 deg, 100% utilisation)
* VDDA2P5 (2.5V): 135.18mA (25 deg, 100% utilisation)
* VDDA1P0 (1V): 124.66mA (105 deg)

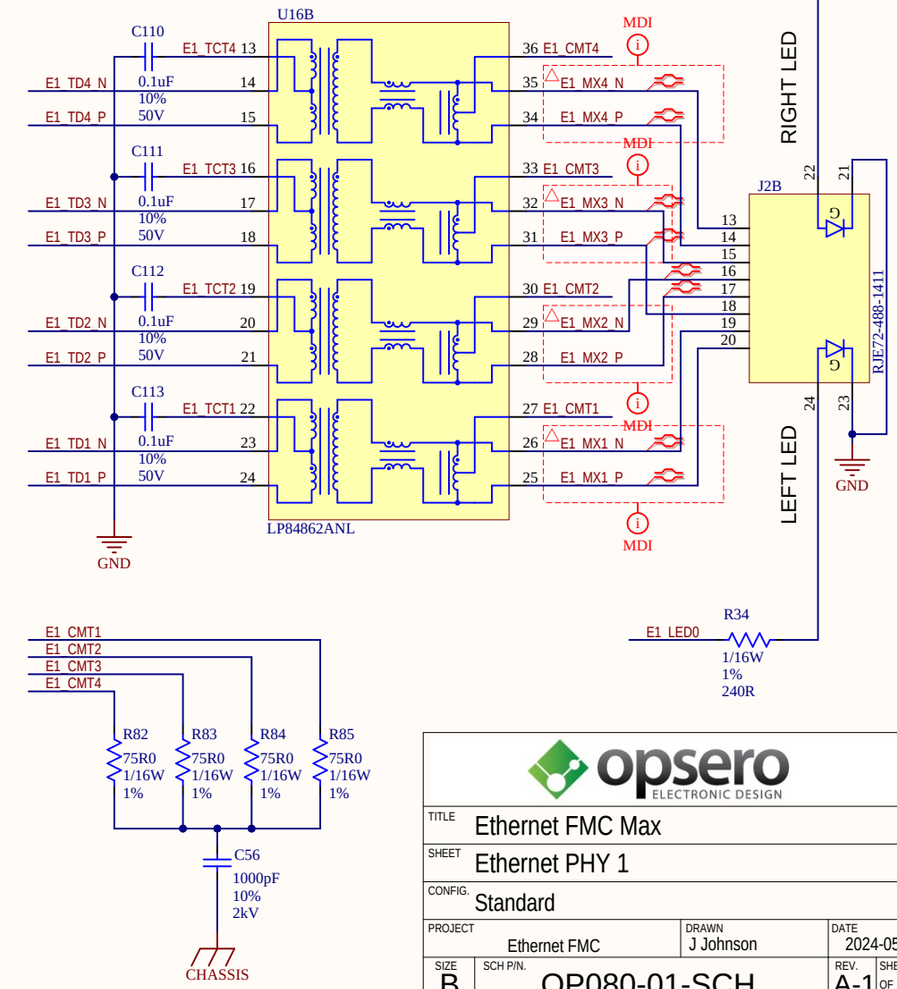
Routing note:
* MDI traces must be 50R to ground and 100R differential impedance
* MDI traces no longer than 2000mils
* MDI traces length matched to 20mils

Supply decoupling



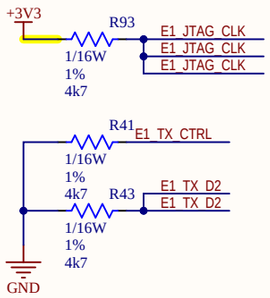




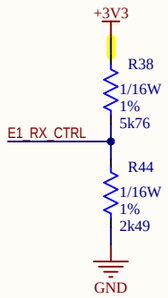


Routing notes:
* SGMII pairs must be routed with 100R differential impedance
* Skew within a pair must be matched to 30mils

Pullups and pulldowns for unused inputs



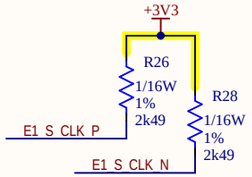
RX_CTRL Strap:
MODE 3 - 5k76 up, 2k49 down
Autoneg disable = 0

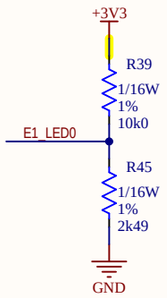


PHY addr = 0011

RX_D0 (S_CLK_P) Strap:
MODE 4 - 2k49 pullups
PHY addr [1:0] = 11

RX_D2 (S_OUT_P) Strap:
MODE 1 - no resistors
PHY addr [3:2] = 00





LED_0 Strap:
MODE 2 - 10K up, 2k49 down
Mirror Enable = 0
SGMII Enable = 1

opsero ELECTRONIC DESIGN

TITLE	Ethernet FMC Max
SHEET	Ethernet PHY 1
CONFIG.	Standard
PROJECT	Ethernet FMC
DRAWN	J Johnson
DATE	2024-05-24
SIZE	B
SCH P/N.	OP080-01-SCH.
REV.	A-1
SHEET OF	4 7

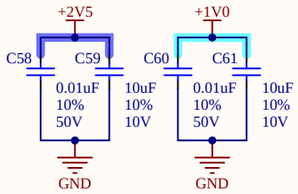
REV.	DESCRIPTION	DATE	APPROVED
A-1	First revision	2024-05-24	J Johnson

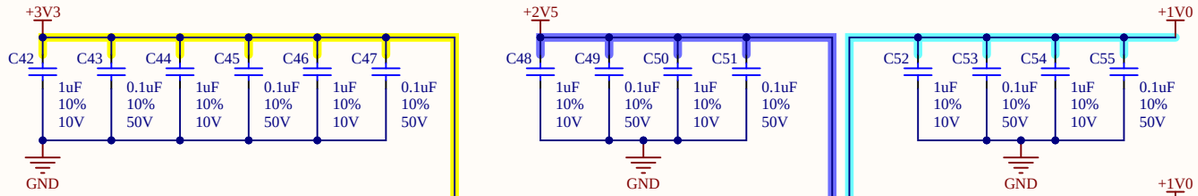
Expected maximum power consumption according to SNLA241:

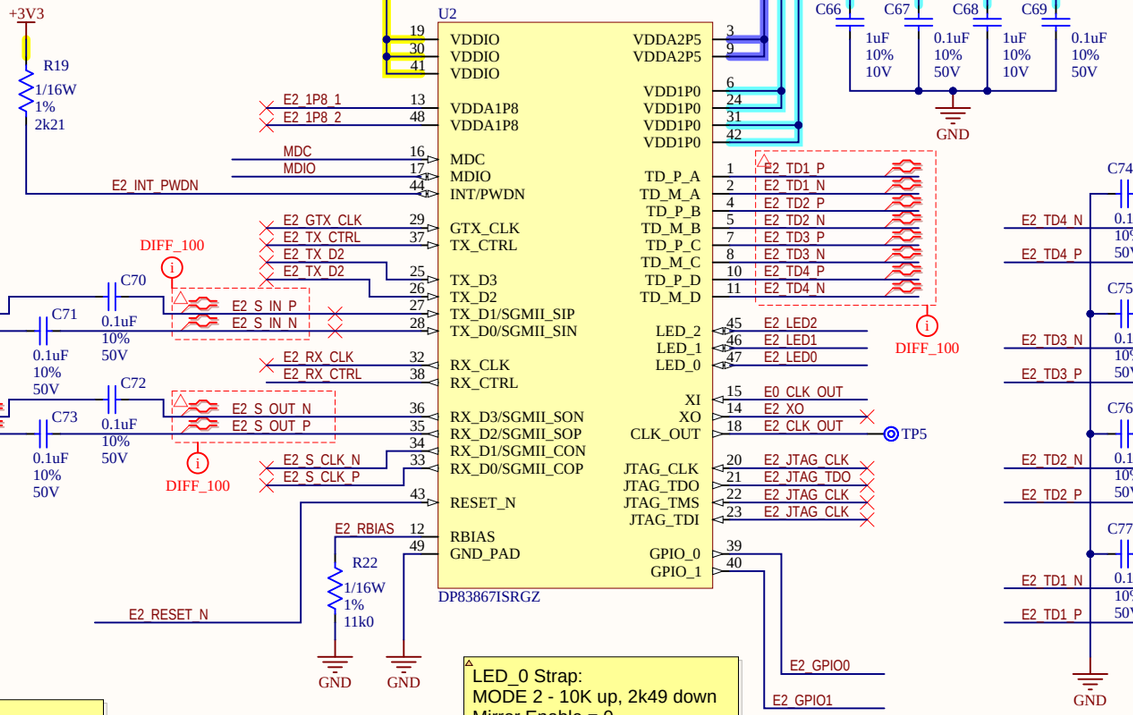
* VDDIO (3.3V): 58.72mA (25 deg, 100% utilisation)
* VDDA2P5 (2.5V): 135.18mA (25 deg, 100% utilisation)
* VDDA1P0 (1V): 124.66mA (105 deg)

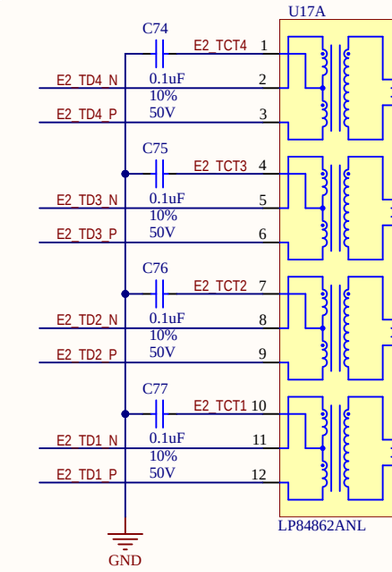
Routing note:
* MDI traces must be 50R to ground and 100R differential impedance
* MDI traces no longer than 2000mils
* MDI traces length matched to 20mils

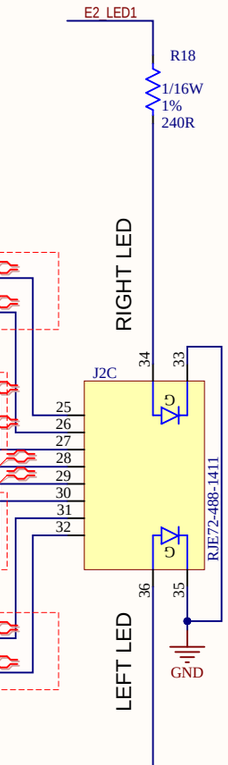
Supply decoupling











Routing notes:
* SGMII pairs must be routed with 100R differential impedance
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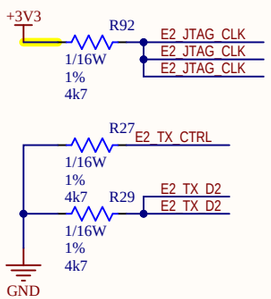
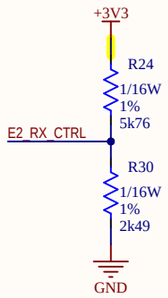
Pullups and pulldowns for unused inputs



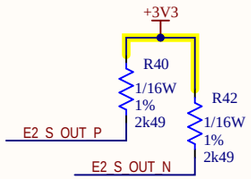
RX_CTRL Strap:
MODE 3 - 5k76 up, 2k49 down
Autoneg disable = 0

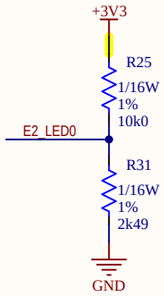


PHY addr = 1100

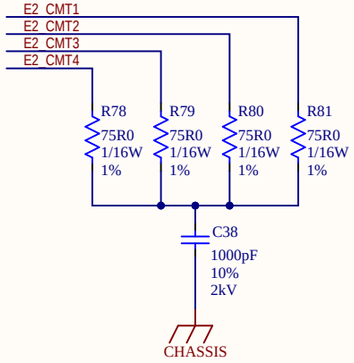
RX_D0 (S_CLK_P) Strap:
MODE 1 - no resistors
PHY addr [1:0] = 00

RX_D2 (S_OUT_P) Strap:
MODE 4 - 2k49 pullups
PHY addr [3:2] = 11





LED_0 Strap:
MODE 2 - 10K up, 2k49 down
Mirror Enable = 0
SGMII Enable = 1



opsero ELECTRONIC DESIGN

TITLE	Ethernet FMC Max
SHEET	Ethernet PHY 2
CONFIG.	Standard
PROJECT	Ethernet FMC
DRAWN	J Johnson
DATE	2024-05-24
SIZE	B
SCH P/N.	OP080-01-SCH.
REV.	A-1
SHEET OF	5 7

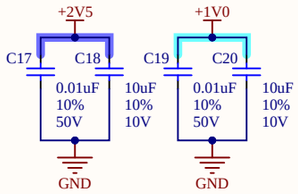
REV.	DESCRIPTION	DATE	APPROVED
A-1	First revision	2024-05-24	J Johnson

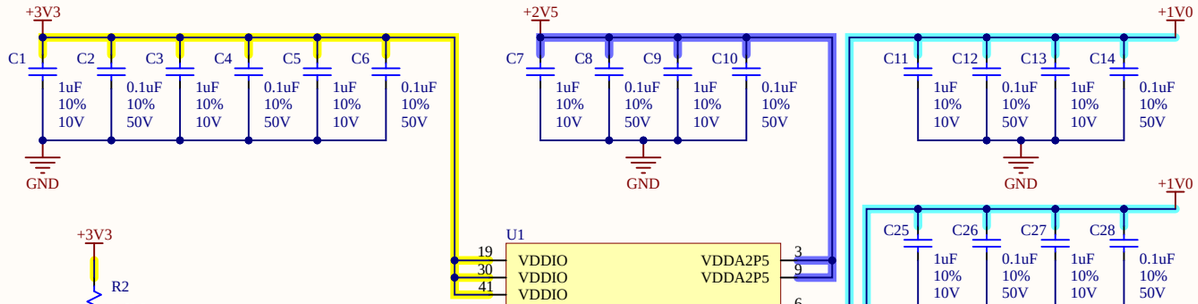
Expected maximum power consumption according to SNLA241:

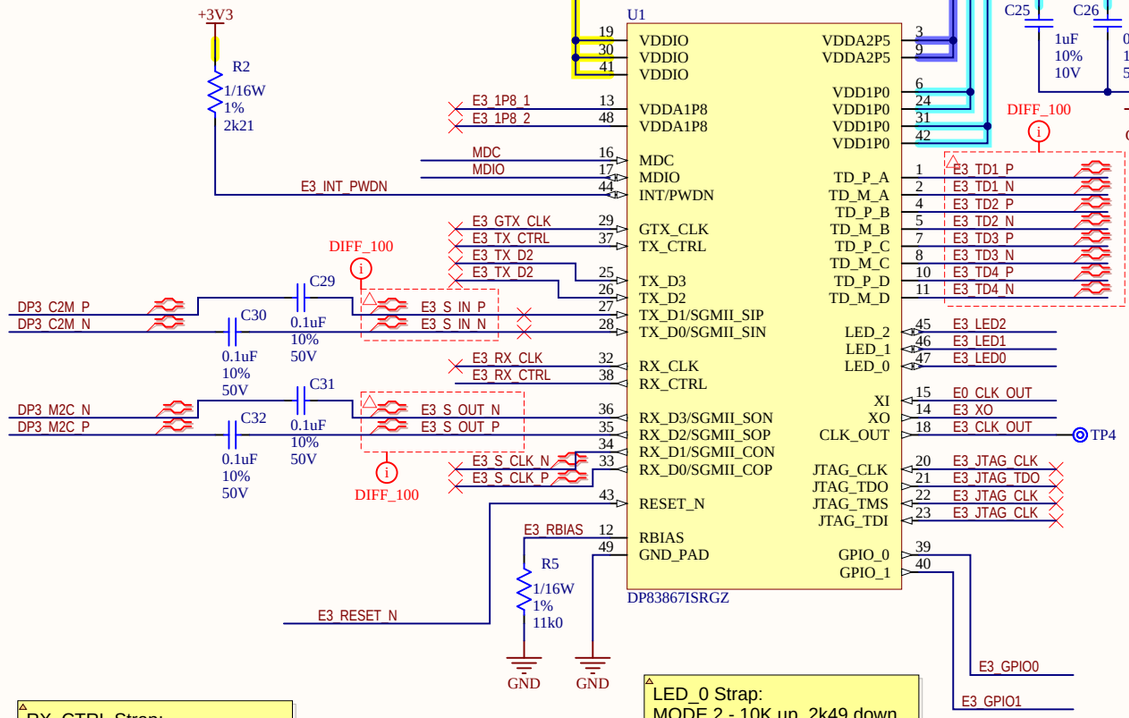
* VDDIO (3.3V): 58.72mA (25 deg, 100% utilisation)
* VDDA2P5 (2.5V): 135.18mA (25 deg, 100% utilisation)
* VDDA1P0 (1V): 124.66mA (105 deg)

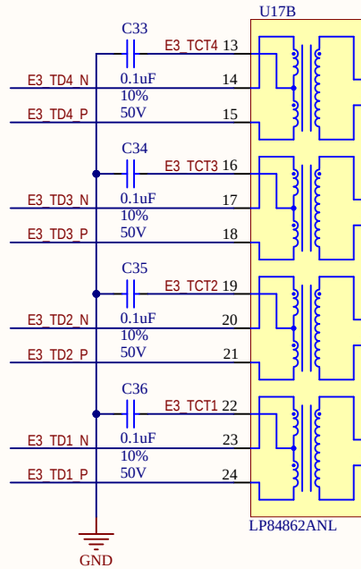
Routing note:
* MDI traces must be 50R to ground and 100R differential impedance
* MDI traces no longer than 2000mils
* MDI traces length matched to 20mils

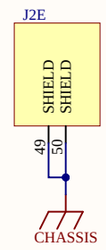
Supply decoupling

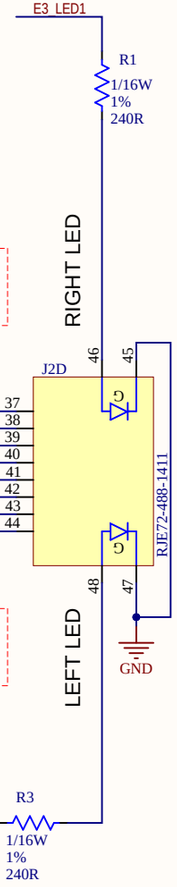






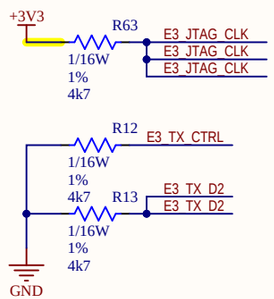




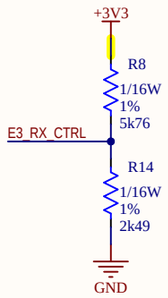


Routing notes:
* SGMII pairs must be routed with 100R differential impedance
* Skew within a pair must be matched to 30mils

Pullups and pulldowns for unused inputs



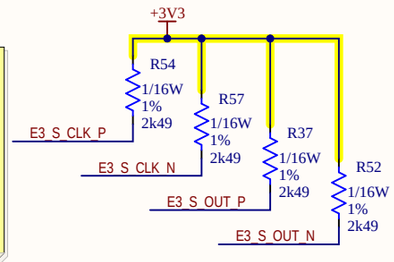
RX_CTRL Strap:
MODE 3 - 5k76 up, 2k49 down
Autoneg disable = 0



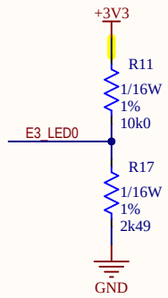
PHY addr = 1111

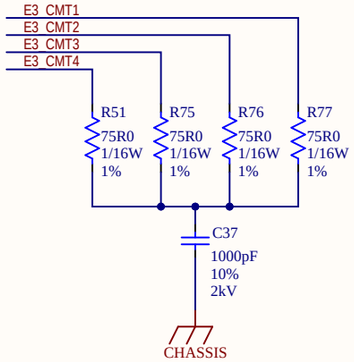
RX_D0 (S_CLK_P) Strap:
MODE 4 - 2k49 pullups
PHY addr [1:0] = 11

RX_D2 (S_OUT_P) Strap:
MODE 4 - 2k49 pullups
PHY addr [3:2] = 11



LED_0 Strap:
MODE 2 - 10K up, 2k49 down
Mirror Enable = 0
SGMII Enable = 1





opsero ELECTRONIC DESIGN

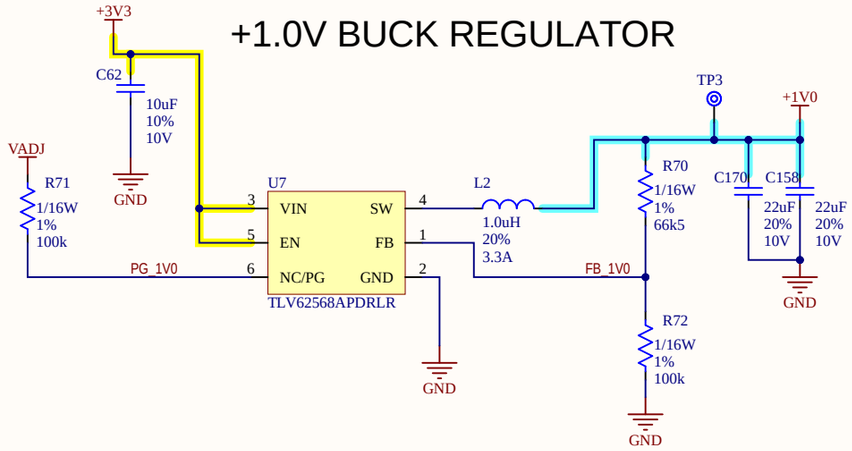
TITLE	Ethernet FMC Max
SHEET	Ethernet PHY 3
CONFIG.	Standard
PROJECT	Ethernet FMC
DRAWN	J Johnson
DATE	2024-05-24
SIZE	B
SCH P/N.	OP080-01-SCH.
REV.	A-1
SHEET OF	6 7

REV.	DESCRIPTION	DATE	APPROVED
A-1	First revision	2024-05-24	J Johnson

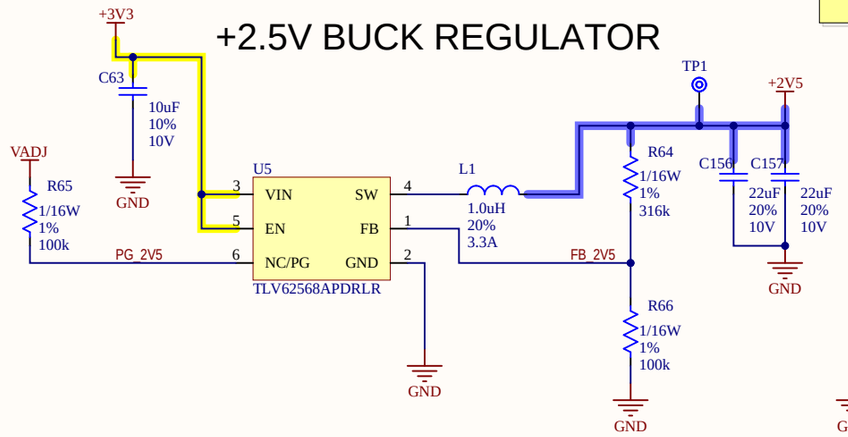
Power supply sequencing:

When using the DP83867 in two-supply mode, there are no power sequencing requirements.

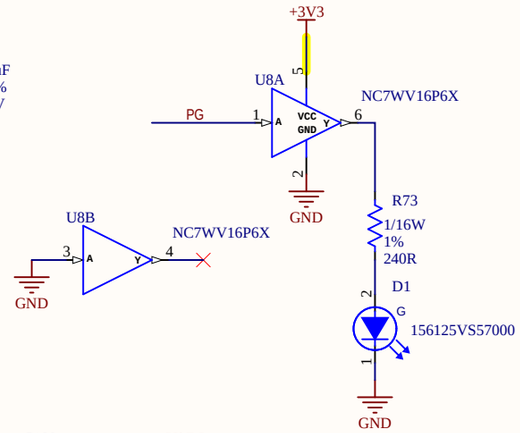
+1.0V BUCK REGULATOR



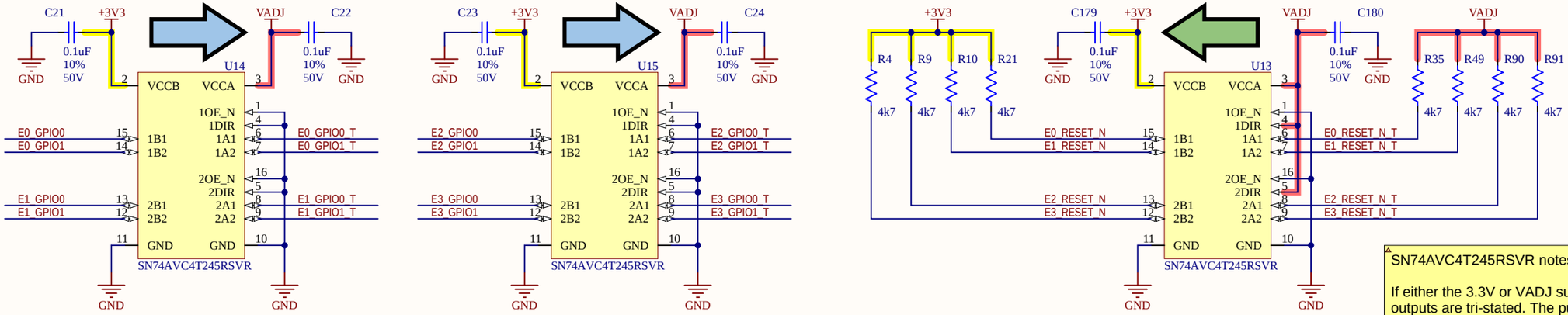
+2.5V BUCK REGULATOR



POWER GOOD LED



VOLTAGE TRANSLATION



DIR INPUT FLOW

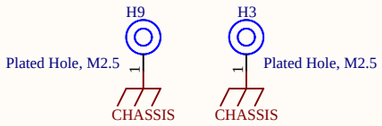
LOW	B -> A
HIGH	A -> B

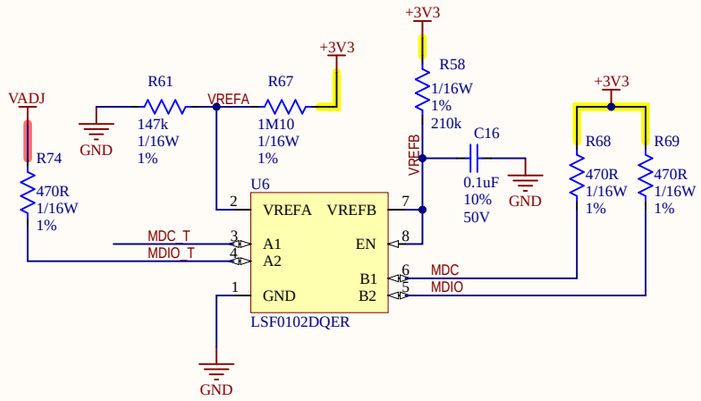
SN74AVC4T245RSVR notes:

If either the 3.3V or VADJ supply is at ZERO, the outputs are tri-stated. The pull-up resistors on the 3.3V side ensure that the PHYs are released from reset even when VADJ is not enabled.

If the reset outputs are tri-stated by the FPGA, the VADJ side pull-ups ensure that the inputs are not floating and that the PHYs are released from reset.

MOUNTING HOLES





TITLE	Ethernet FMC Max		
SHEET	Power supplies		
CONFIG.	Standard		
PROJECT	Ethernet FMC	DRAWN J Johnson	DATE 2024-05-24
SIZE B	SCH P/N. OP080-01-SCH.	REV. A-1	SHEET 7 OF 7