REV.	DESCRIPTION	DATE	APPROVED
F.1	Increased PCB rev for RJ45 footprint optimization	2019-12-17	J Johnson

F1 Fiducial

F2 Fiducial

F3 Fiducial

S1

Standoff, Hex, 10mm, M2.5

S2

Standoff, Hex, 10mm, M2.5

H1 Plated Hole, M2

H3 Plated Hole, M2.5

H11 Plated Hole, M2

H9 Plated Hole, M2.5

GND

U_EthernetPHY0
EthernetPHY0.SchDoc

U_FMCConnector
FMCConnector.SchDoc

E0_RESET_N	E0_RESET_N
E0_RX_CLK	E0_RX_CLK
E0_RX_CTRL	E0_RX_CTRL
E0_RXD0	E0_RXD0
E0_RXD1	E0_RXD1
E0_RXD2	E0_RXD2
E0_RXD3	E0_RXD3
E0_TXD0	E0_TXD0
E0_TXD1	E0_TXD1
E0_TXD2	E0_TXD2
E0_TXD3	E0_TXD3
E0_TX_CLK	E0_TX_CLK
E0_TX_CTRL	E0_TX_CTRL
E0_MDIO	E0_MDIO
E0_MDC	E0_MDC

U_EthernetPHY1
EthernetPHY1.SchDoc

E1_RESET_N	E1_RESET_N
E1_RX_CLK	E1_RX_CLK
E1_RX_CTRL	E1_RX_CTRL
E1_RXD0	E1_RXD0
E1_RXD1	E1_RXD1
E1_RXD2	E1_RXD2
E1_RXD3	E1_RXD3
E1_TXD0	E1_TXD0
E1_TXD1	E1_TXD1
E1_TXD2	E1_TXD2
E1_TXD3	E1_TXD3
E1_TX_CLK	E1_TX_CLK
E1_TX_CTRL	E1_TX_CTRL
E1_MDIO	E1_MDIO
E1_MDC	E1_MDC

U_EthernetPHY2
EthernetPHY2.SchDoc

E2_RESET_N	E2_RESET_N
E2_RX_CLK	E2_RX_CLK
E2_RX_CTRL	E2_RX_CTRL
E2_RXD0	E2_RXD0
E2_RXD1	E2_RXD1
E2_RXD2	E2_RXD2
E2_RXD3	E2_RXD3
E2_TXD0	E2_TXD0
E2_TXD1	E2_TXD1
E2_TXD2	E2_TXD2
E2_TXD3	E2_TXD3
E2_TX_CLK	E2_TX_CLK
E2_TX_CTRL	E2_TX_CTRL
E2_MDIO	E2_MDIO
E2_MDC	E2_MDC

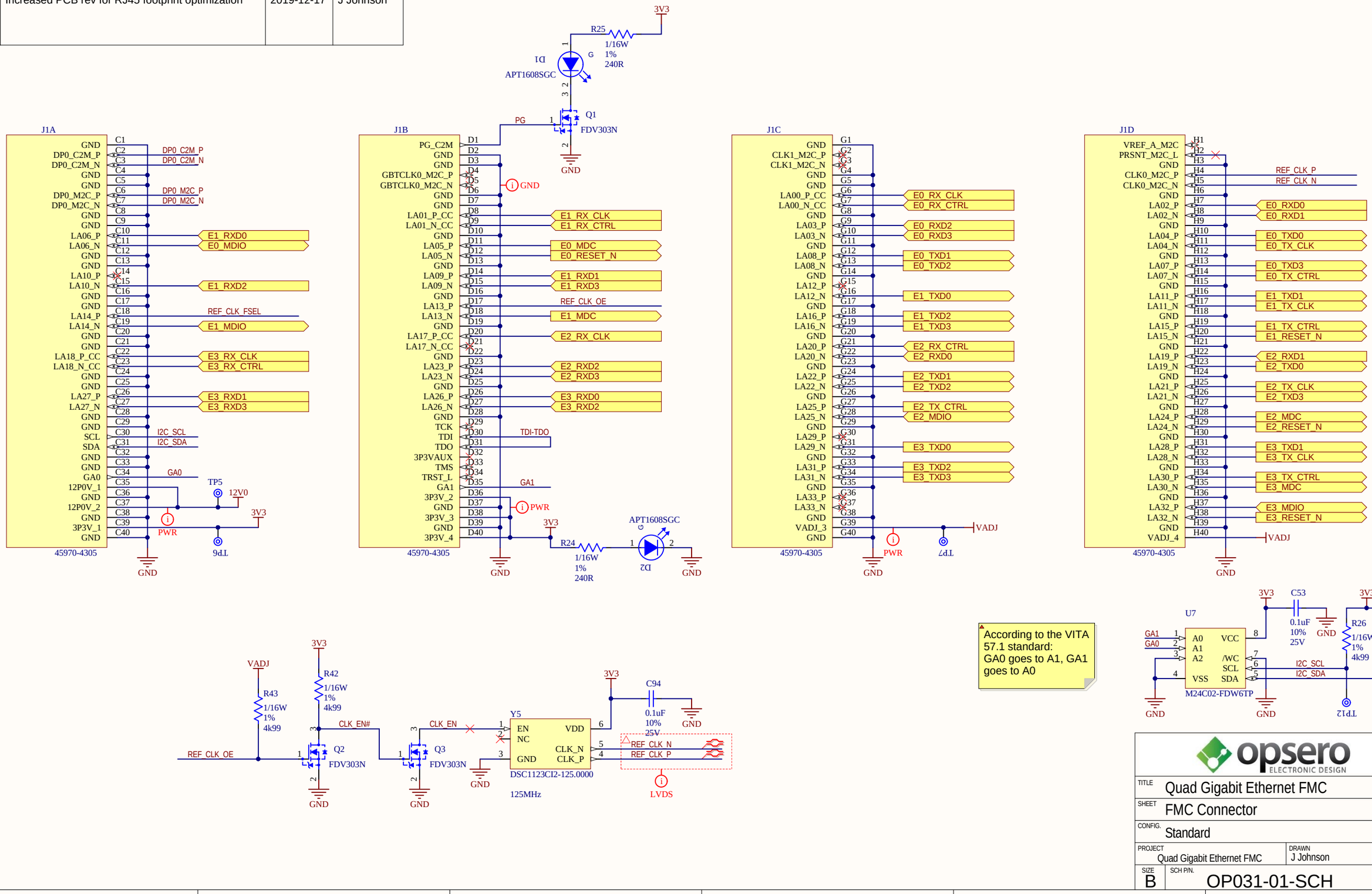
U_EthernetPHY3
EthernetPHY3.SchDoc

E3_RESET_N	E3_RESET_N
E3_RX_CLK	E3_RX_CLK
E3_RX_CTRL	E3_RX_CTRL
E3_RXD0	E3_RXD0
E3_RXD1	E3_RXD1
E3_RXD2	E3_RXD2
E3_RXD3	E3_RXD3
E3_TXD0	E3_TXD0
E3_TXD1	E3_TXD1
E3_TXD2	E3_TXD2
E3_TXD3	E3_TXD3
E3_TX_CLK	E3_TX_CLK
E3_TX_CTRL	E3_TX_CTRL
E3_MDIO	E3_MDIO
E3_MDC	E3_MDC

opsero ELECTRONIC DESIGN

TITLE	Quad Gigabit Ethernet FMC		
SHEET	Top level		
CONFIG.	Standard		
PROJECT	Quad Gigabit Ethernet FMC	DRAWN J Johnson	DATE 2014-09-11
SIZE B	SCH P/N. OP031-01-SCH	REV. F.1	SHEET 1 OF 6

REV.	DESCRIPTION	DATE	APPROVED
F.1	Increased PCB rev for RJ45 footprint optimization	2019-12-17	J Johnson



According to the VITA 57.1 standard:
GA0 goes to A1, GA1 goes to A0

opsero ELECTRONIC DESIGN

TITLE	Quad Gigabit Ethernet FMC
SHEET	FMC Connector
CONFIG.	Standard
PROJECT	Quad Gigabit Ethernet FMC
DRAWN	J Johnson
DATE	2014-09-11
SIZE	B
SCH P/N.	OP031-01-SCH
REV.	F.1
SHEET OF	2 6

REV.	DESCRIPTION	DATE	APPROVED
F.1	Increased PCB rev for RJ45 footprint optimization	2019-12-17	J Johnson

VDDO (VADJ) supplies MDC, MDIO, RESET_N, LED[2:0], CONFIG, CLK125 and RGMII pins, therefore no voltage conversion required to the FMC connector.

The standard configuration is for a VADJ voltage of 2.5V. For a VADJ of 3.3V or 1.8V, hardware modifications are required.

For VDDO (VADJ) of 3.3V, the CONFIG pin should be tied to GND and the 0R resistor removed. The 88E1510 device will support a VDDO (VADJ) of 3.3V or 2.5V, however be aware that the Xilinx Series 7 devices only support 2.5V or 1.8V RGMII.

For VDDO (VADJ) of 1.8V, the 88E1518 device should be used.

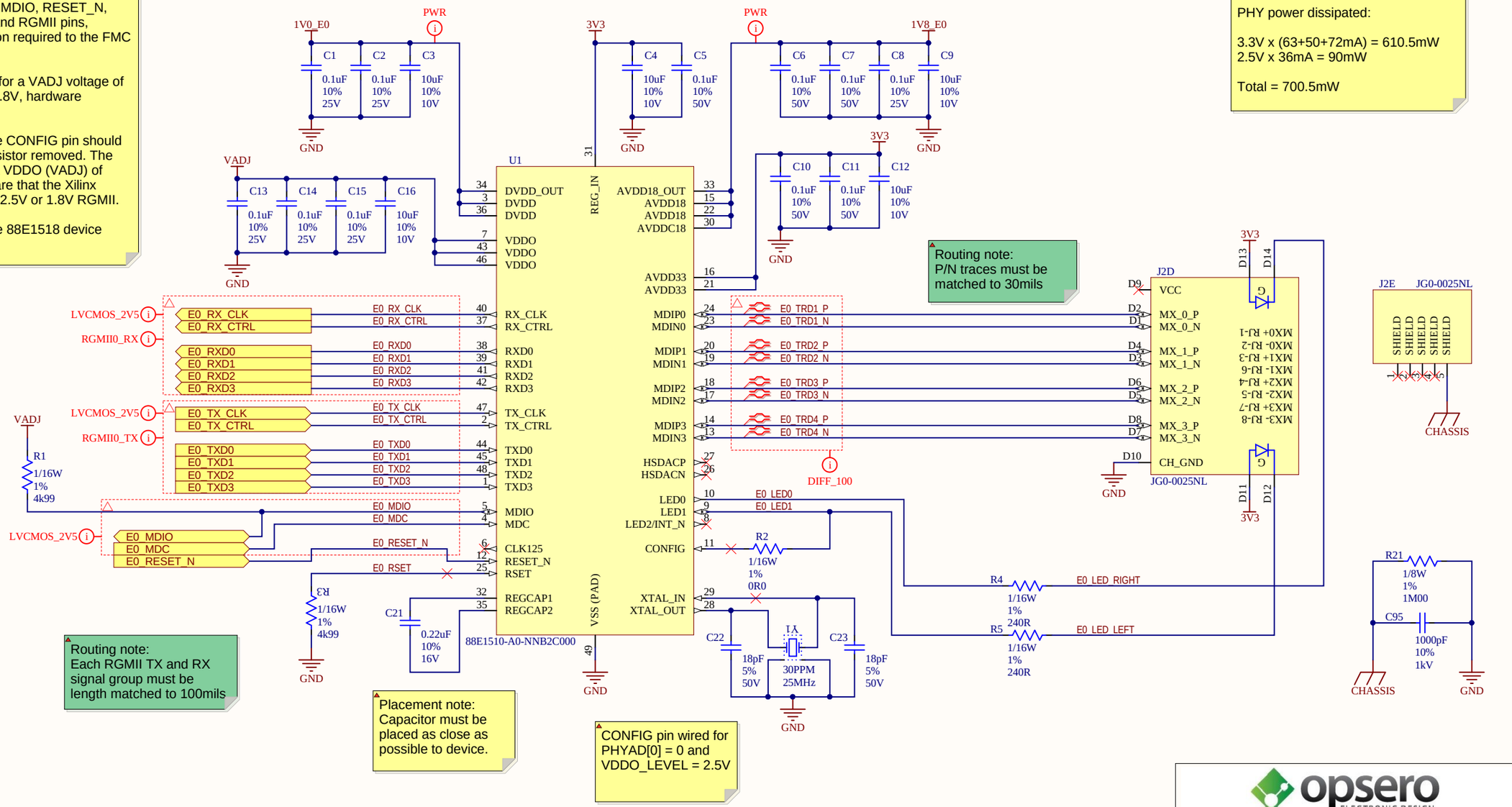
PHY current consumption:

1.8V supply: 63mA
3.3V supply: 50mA
1.0V supply: 72mA
2.5V supply: 36mA

PHY power dissipated:

3.3V x (63+50+72mA) = 610.5mW
2.5V x 36mA = 90mW

Total = 700.5mW



TITLE	Quad Gigabit Ethernet FMC		
SHEET	Ethernet PHY 0		
CONFIG.	Standard		
PROJECT	Quad Gigabit Ethernet FMC	DRAWN: J Johnson	DATE: 2014-09-11
SIZE: B	SCH P/N: OP031-01-SCH	REV.: F.1	SHEET OF: 3 6

REV.	DESCRIPTION	DATE	APPROVED
F.1	Increased PCB rev for RJ45 footprint optimization	2019-12-17	J Johnson

VDDO (VADJ) supplies MDC, MDIO, RESET_N, LED[2:0], CONFIG, CLK125 and RGMII pins, therefore no voltage conversion required to the FMC connector.

The standard configuration is for a VADJ voltage of 2.5V. For a VADJ of 3.3V or 1.8V, hardware modifications are required.

For VDDO (VADJ) of 3.3V, the CONFIG pin should be tied to GND and the 0R resistor removed. The 88E1510 device will support a VDDO (VADJ) of 3.3V or 2.5V, however be aware that the Xilinx Series 7 devices only support 2.5V or 1.8V RGMII.

For VDDO (VADJ) of 1.8V, the 88E1518 device should be used.

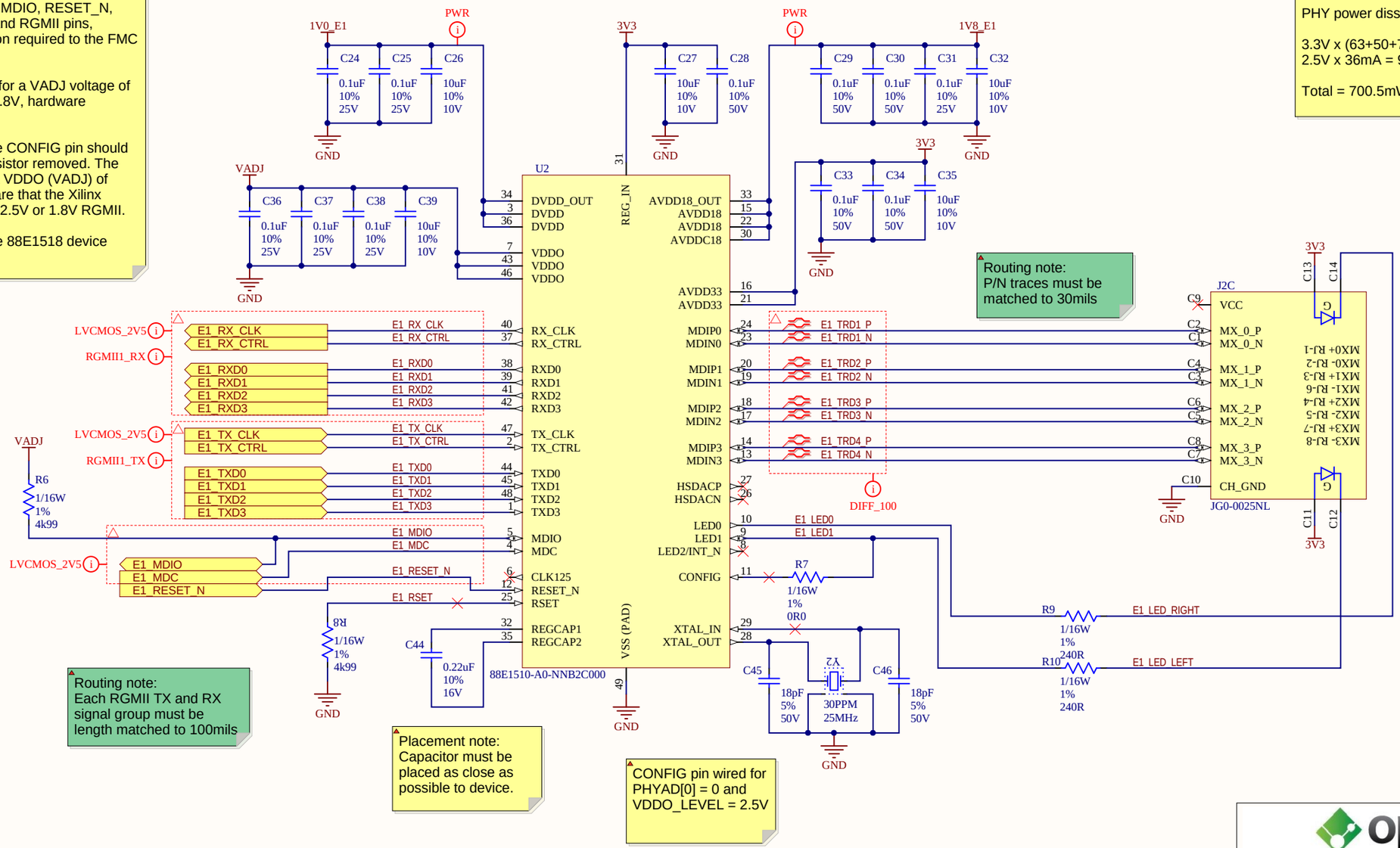
PHY current consumption:

1.8V supply: 63mA
3.3V supply: 50mA
1.0V supply: 72mA
2.5V supply: 36mA

PHY power dissipated:

3.3V x (63+50+72mA) = 610.5mW
2.5V x 36mA = 90mW

Total = 700.5mW



Routing note:
Each RGMII TX and RX signal group must be length matched to 100mils

Placement note:
Capacitor must be placed as close as possible to device.

CONFIG pin wired for PHYAD[0] = 0 and VDDO_LEVEL = 2.5V

Routing note:
P/N traces must be matched to 30mils

opsero ELECTRONIC DESIGN

TITLE	Quad Gigabit Ethernet FMC
SHEET	Ethernet PHY 1
CONFIG.	Standard
PROJECT	Quad Gigabit Ethernet FMC
DRAWN	J Johnson
DATE	2014-09-11
SIZE	B
SCH P/N.	OP031-01-SCH
REV.	F.1
SHEET OF	4 6

REV.	DESCRIPTION	DATE	APPROVED
F.1	Increased PCB rev for RJ45 footprint optimization	2019-12-17	J Johnson

VDDO (VADJ) supplies MDC, MDIO, RESET_N, LED[2:0], CONFIG, CLK125 and RGMII pins, therefore no voltage conversion required to the FMC connector.

The standard configuration is for a VADJ voltage of 2.5V. For a VADJ of 3.3V or 1.8V, hardware modifications are required.

For VDDO (VADJ) of 3.3V, the CONFIG pin should be tied to GND and the 0R resistor removed. The 88E1510 device will support a VDDO (VADJ) of 3.3V or 2.5V, however be aware that the Xilinx Series 7 devices only support 2.5V or 1.8V RGMII.

For VDDO (VADJ) of 1.8V, the 88E1518 device should be used.

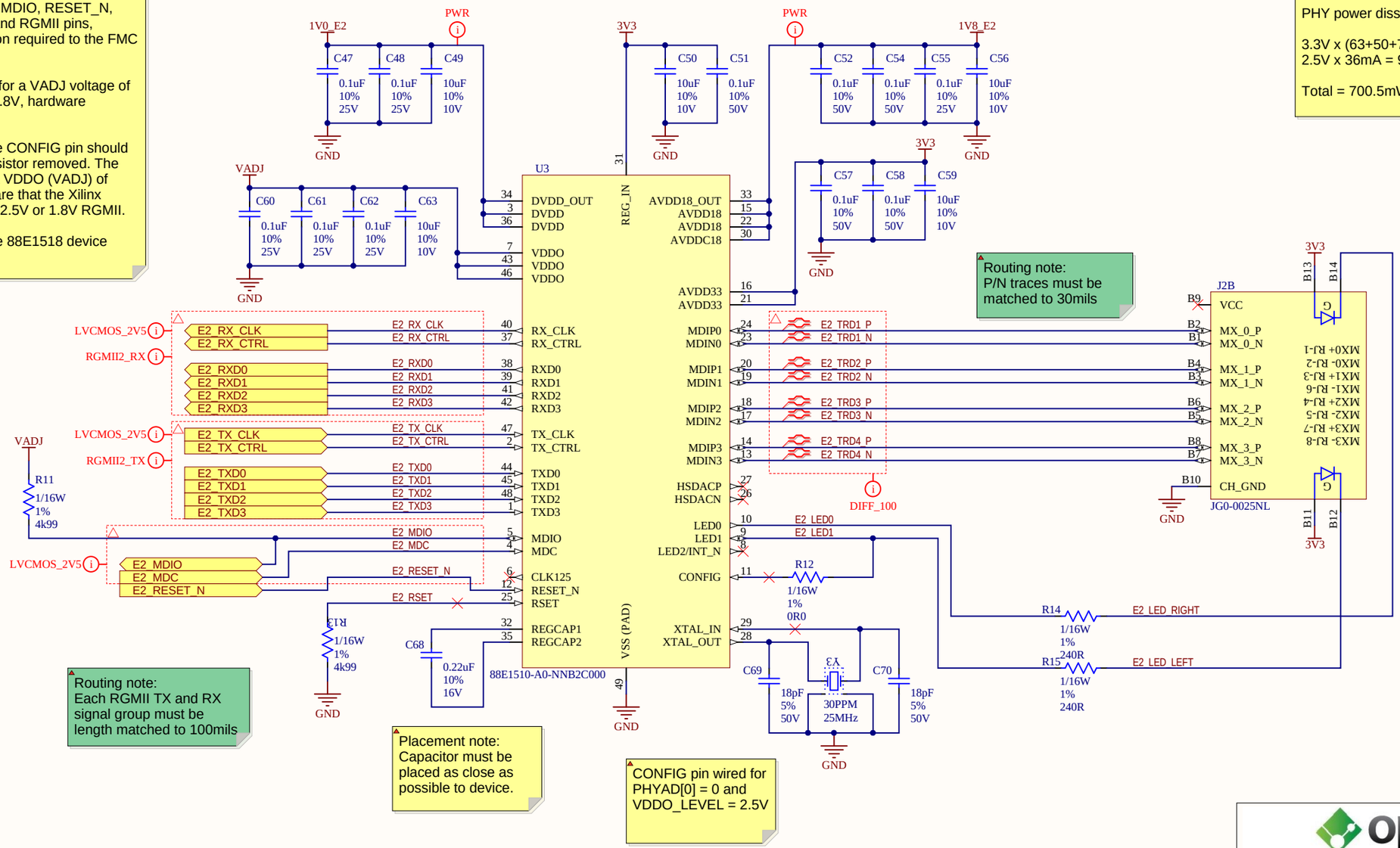
PHY current consumption:

1.8V supply: 63mA
3.3V supply: 50mA
1.0V supply: 72mA
2.5V supply: 36mA

PHY power dissipated:

3.3V x (63+50+72mA) = 610.5mW
2.5V x 36mA = 90mW

Total = 700.5mW



Routing note:
P/N traces must be matched to 30mils

Routing note:
Each RGMII TX and RX signal group must be length matched to 100mils

Placement note:
Capacitor must be placed as close as possible to device.

CONFIG pin wired for PHYAD[0] = 0 and VDDO_LEVEL = 2.5V

opsero ELECTRONIC DESIGN

TITLE	Quad Gigabit Ethernet FMC
SHEET	Ethernet PHY 2
CONFIG.	Standard
PROJECT	Quad Gigabit Ethernet FMC
DRAWN	J Johnson
DATE	2014-09-11
SIZE	B
SCH P/N.	OP031-01-SCH
REV.	F.1
SHEET OF	5 6

REV.	DESCRIPTION	DATE	APPROVED
F.1	Increased PCB rev for RJ45 footprint optimization	2019-12-17	J Johnson

VDDO (VADJ) supplies MDC, MDIO, RESET_N, LED[2:0], CONFIG, CLK125 and RGMII pins, therefore no voltage conversion required to the FMC connector.

The standard configuration is for a VADJ voltage of 2.5V. For a VADJ of 3.3V or 1.8V, hardware modifications are required.

For VDDO (VADJ) of 3.3V, the CONFIG pin should be tied to GND and the 0R resistor removed. The 88E1510 device will support a VDDO (VADJ) of 3.3V or 2.5V, however be aware that the Xilinx Series 7 devices only support 2.5V or 1.8V RGMII.

For VDDO (VADJ) of 1.8V, the 88E1518 device should be used.

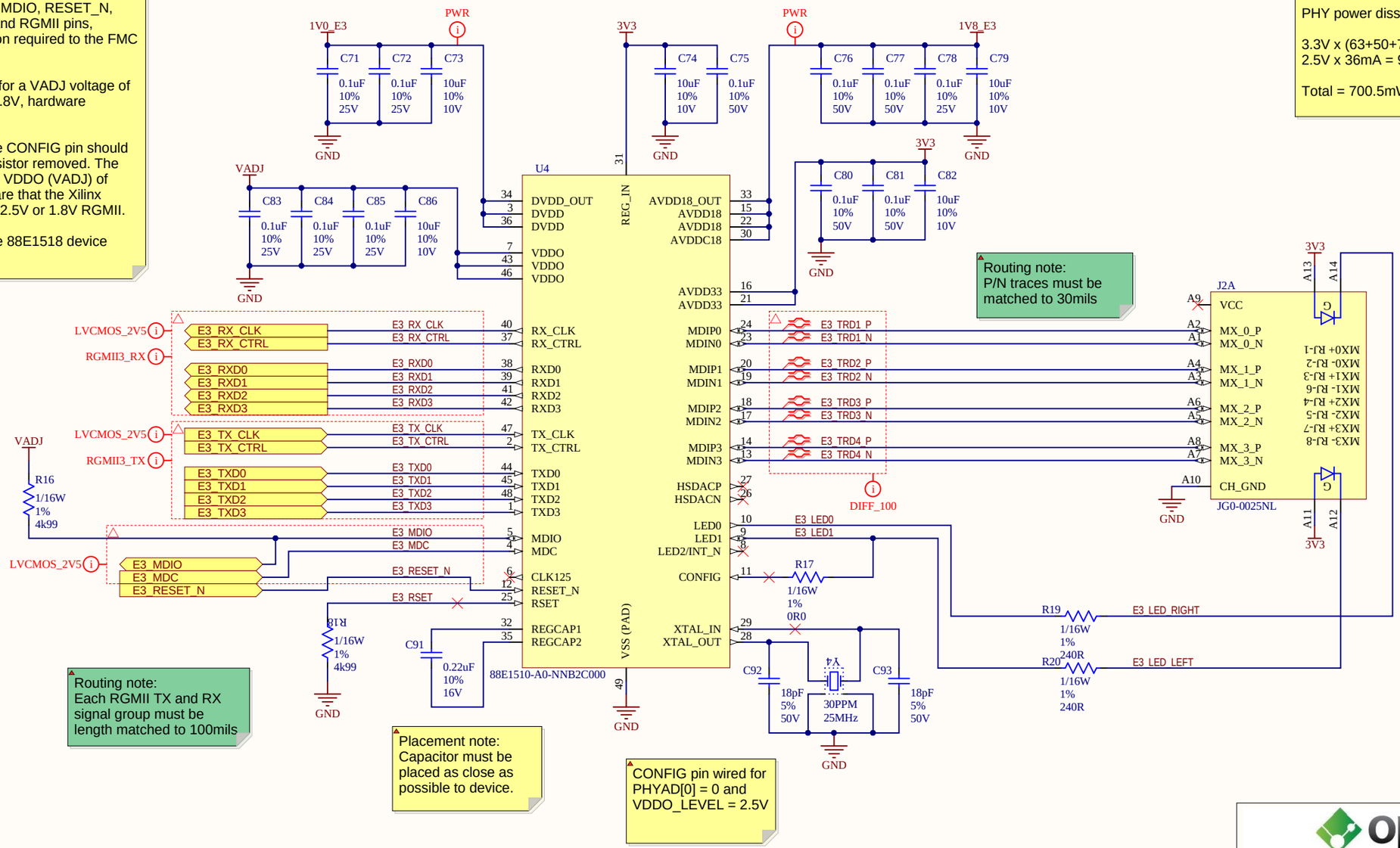
PHY current consumption:

1.8V supply: 63mA
3.3V supply: 50mA
1.0V supply: 72mA
2.5V supply: 36mA

PHY power dissipated:

3.3V x (63+50+72mA) = 610.5mW
2.5V x 36mA = 90mW

Total = 700.5mW



Routing note:
P/N traces must be matched to 30mils

Routing note:
Each RGMII TX and RX signal group must be length matched to 100mils

Placement note:
Capacitor must be placed as close as possible to device.

CONFIG pin wired for PHYAD[0] = 0 and VDDO_LEVEL = 2.5V

opsero ELECTRONIC DESIGN

TITLE	Quad Gigabit Ethernet FMC
SHEET	Ethernet PHY 3
CONFIG.	Standard
PROJECT	Quad Gigabit Ethernet FMC
DRAWN	J Johnson
DATE	2014-09-11
SIZE	B
SCH P/N.	OP031-01-SCH
REV.	F.1
SHEET OF	6 6