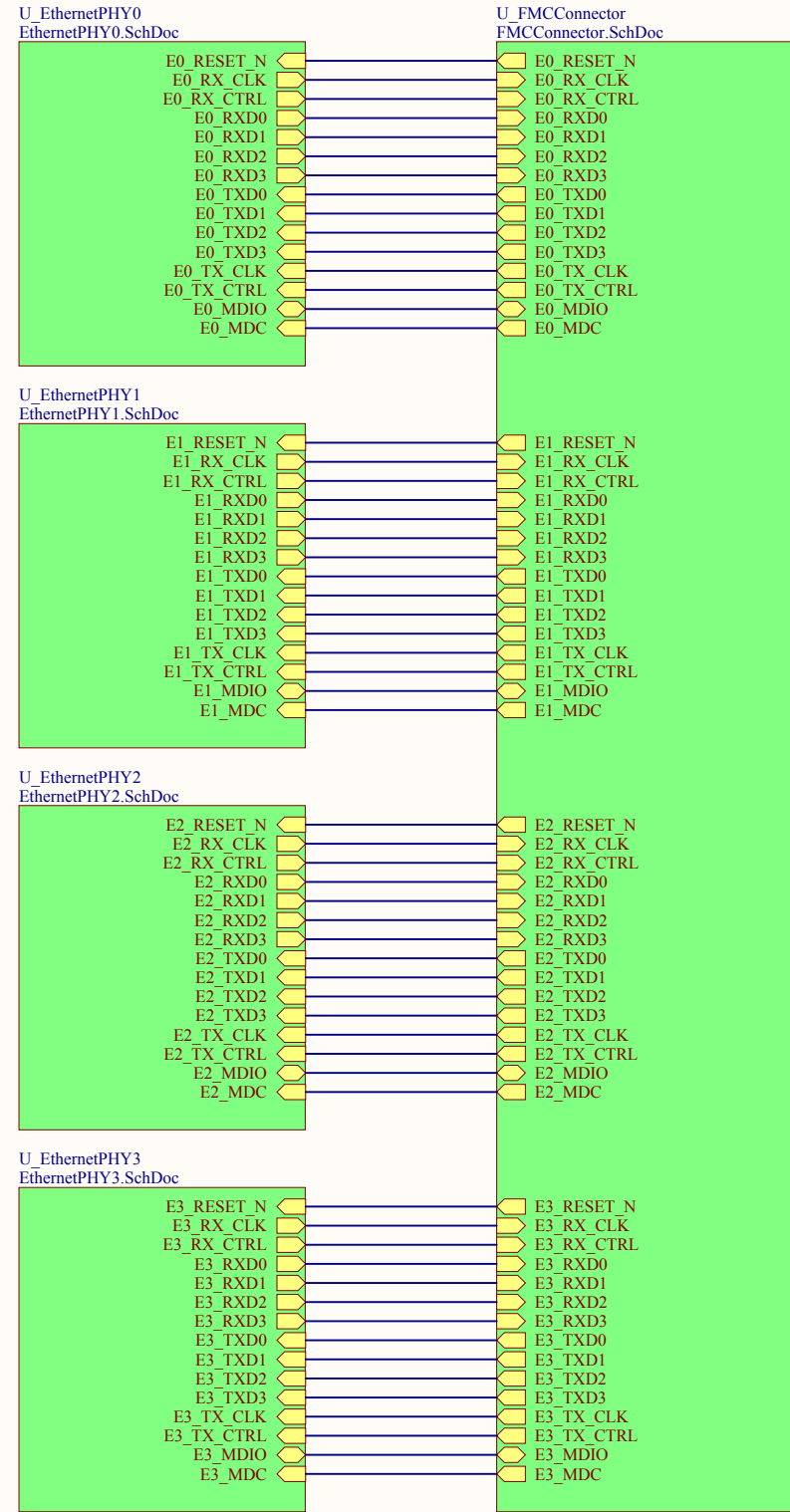
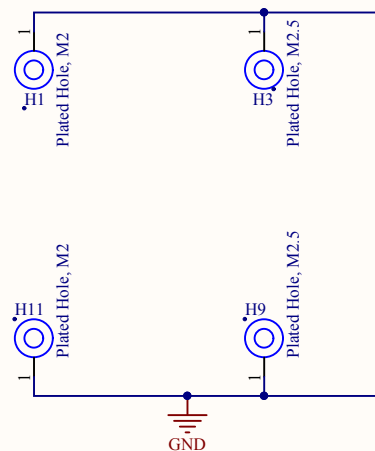
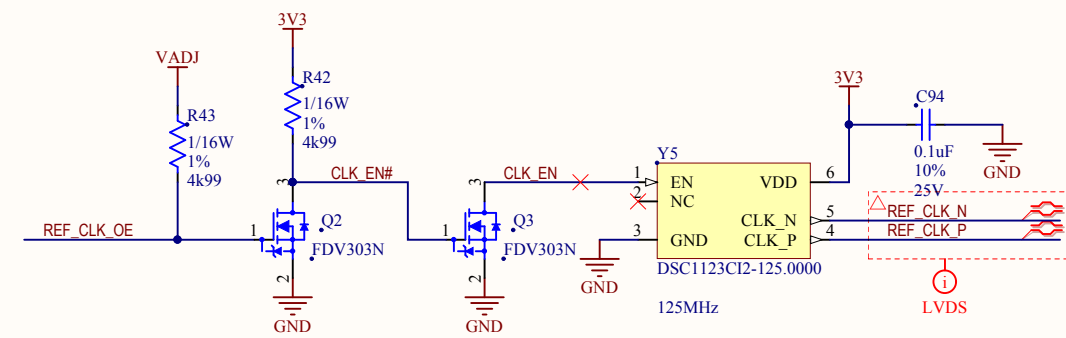
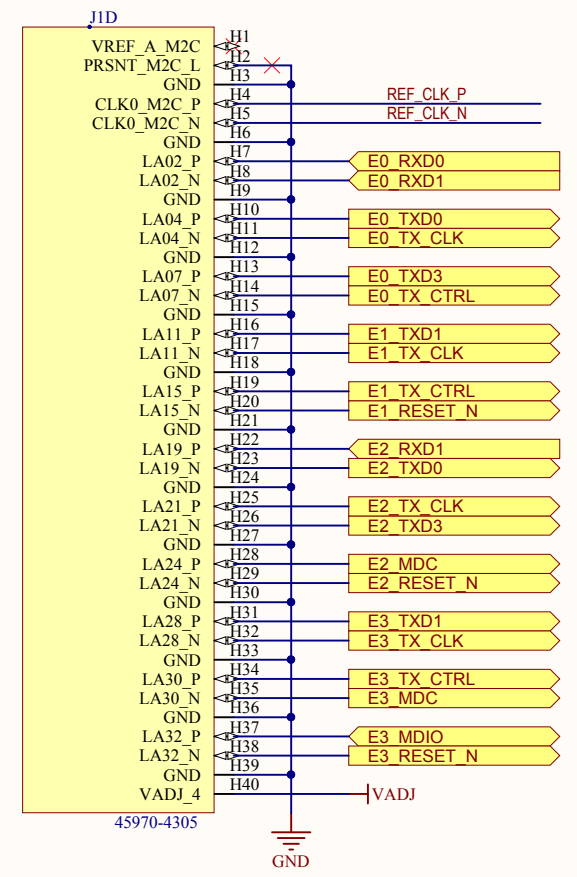
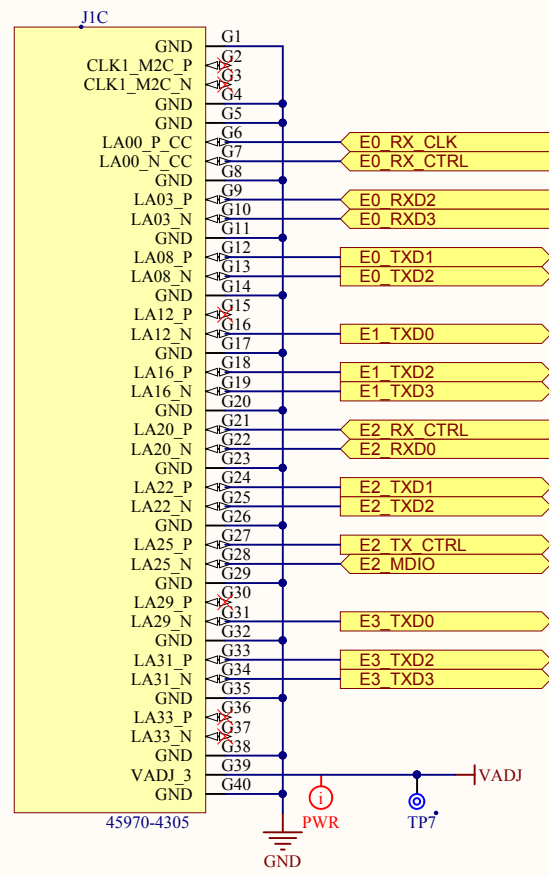
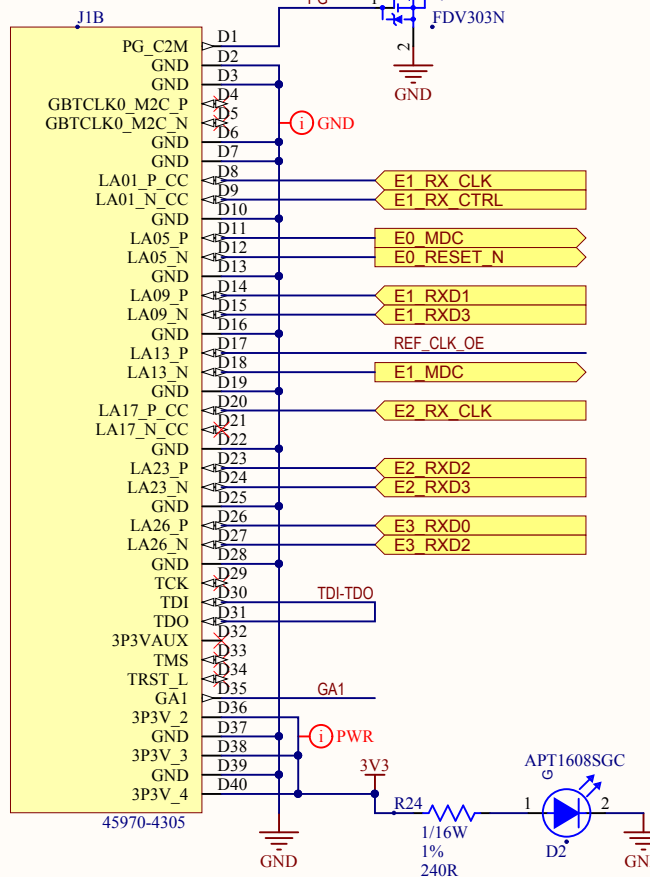
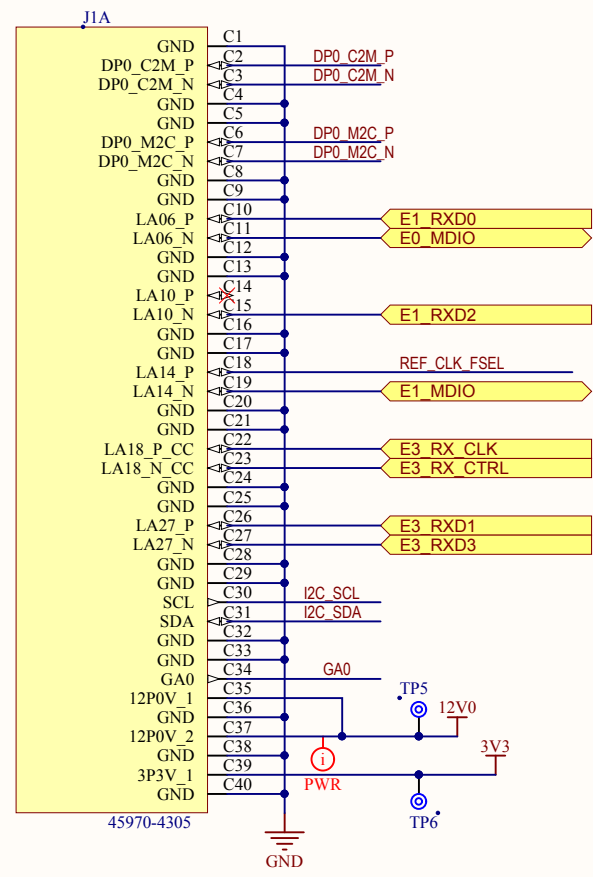
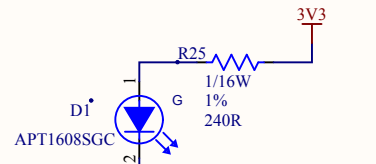


REV.	DESCRIPTION	DATE	APPROVED
E.1	Changed 125MHz oscillator to Micrel part FSEL option removed Added buffer to allow 1.8V CLK_EN	2016-02-06	J Johnson

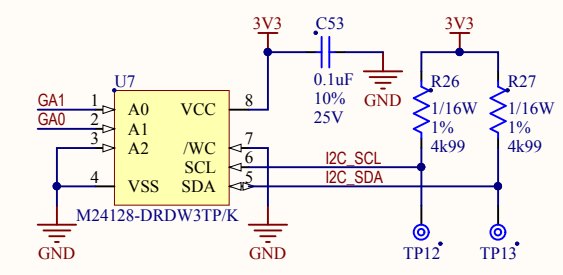


TITLE Quad Gigabit Ethernet FMC			
SHEET Top level			
CONFIG. Standard			
PROJECT	Quad Gigabit Ethernet FMC	DRAWN	J Johnson
DATE	2014-09-11	REV.	E.1
SIZE	SCH P/N.	OP031-01-SCH	SHEET 1 OF 6

REV.	DESCRIPTION	DATE	APPROVED
E.1	Changed 125MHz oscillator to Micrel part FSEL option removed Added buffer to allow 1.8V CLK_EN	2016-02-06	J Johnson



According to the VITA 57.1 standard:  
GA0 goes to A1, GA1 goes to A0



**opsero**  
ELECTRONIC DESIGN

TITLE <b>Quad Gigabit Ethernet FMC</b>		
SHEET <b>FMC Connector</b>		
CONFIG. <b>Standard</b>		
PROJECT Quad Gigabit Ethernet FMC	DRAWN J Johnson	DATE 2014-09-11
SIZE <b>B</b>	SCH P/N. <b>OP031-01-SCH</b>	REV. <b>E.1</b> SHEET OF <b>2</b>

REV.	DESCRIPTION	DATE	APPROVED
E.1	Changed 125MHz oscillator to Micrel part FSEL option removed Added buffer to allow 1.8V CLK_EN	2016-02-06	J Johnson

VDDO (VADJ) supplies MDC, MDIO, RESET\_N, LED[2:0], CONFIG, CLK125 and RGMII pins, therefore no voltage conversion required to the FMC connector.

The standard configuration is for a VADJ voltage of 2.5V. For a VADJ of 3.3V or 1.8V, hardware modifications are required.

For VDDO (VADJ) of 3.3V, the CONFIG pin should be tied to GND and the 0R resistor removed. The 88E1510 device will support a VDDO (VADJ) of 3.3V or 2.5V, however be aware that the Xilinx Series 7 devices only support 2.5V or 1.8V RGMII.

For VDDO (VADJ) of 1.8V, the 88E1518 device should be used.

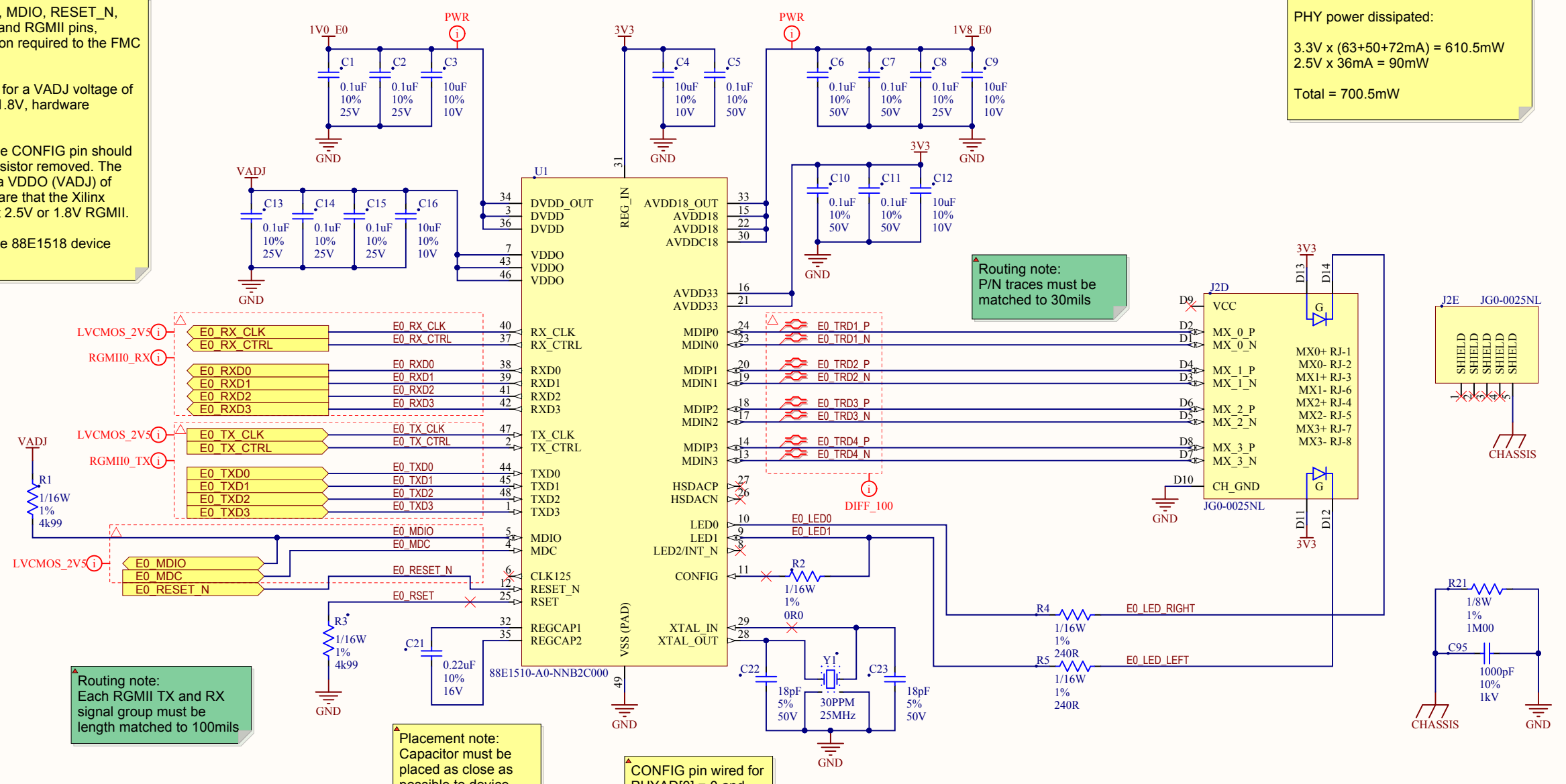
PHY current consumption:

1.8V supply: 63mA  
3.3V supply: 50mA  
1.0V supply: 72mA  
2.5V supply: 36mA

PHY power dissipated:

$3.3V \times (63+50+72mA) = 610.5mW$   
 $2.5V \times 36mA = 90mW$

Total = 700.5mW



Routing note:  
P/N traces must be matched to 30mils

Routing note:  
Each RGMII TX and RX signal group must be length matched to 100mils

Placement note:  
Capacitor must be placed as close as possible to device.

CONFIG pin wired for PHYAD[0] = 0 and VDDO\_LEVEL = 2.5V

TITLE Quad Gigabit Ethernet FMC			
SHEET Ethernet PHY 0			
CONFIG. Standard			
PROJECT	DRAWN	DATE	
Quad Gigabit Ethernet FMC	J Johnson	2014-09-11	
SIZE	SCH P/N.	REV.	SHEET OF
B	OP031-01-SCH	E.1	3 OF 6

REV.	DESCRIPTION	DATE	APPROVED
E.1	Changed 125MHz oscillator to Micrel part FSEL option removed Added buffer to allow 1.8V CLK_EN	2016-02-06	J Johnson

VDDO (VADJ) supplies MDC, MDIO, RESET\_N, LED[2:0], CONFIG, CLK125 and RGMII pins, therefore no voltage conversion required to the FMC connector.

The standard configuration is for a VADJ voltage of 2.5V. For a VADJ of 3.3V or 1.8V, hardware modifications are required.

For VDDO (VADJ) of 3.3V, the CONFIG pin should be tied to GND and the 0R resistor removed. The 88E1510 device will support a VDDO (VADJ) of 3.3V or 2.5V, however be aware that the Xilinx Series 7 devices only support 2.5V or 1.8V RGMII.

For VDDO (VADJ) of 1.8V, the 88E1518 device should be used.

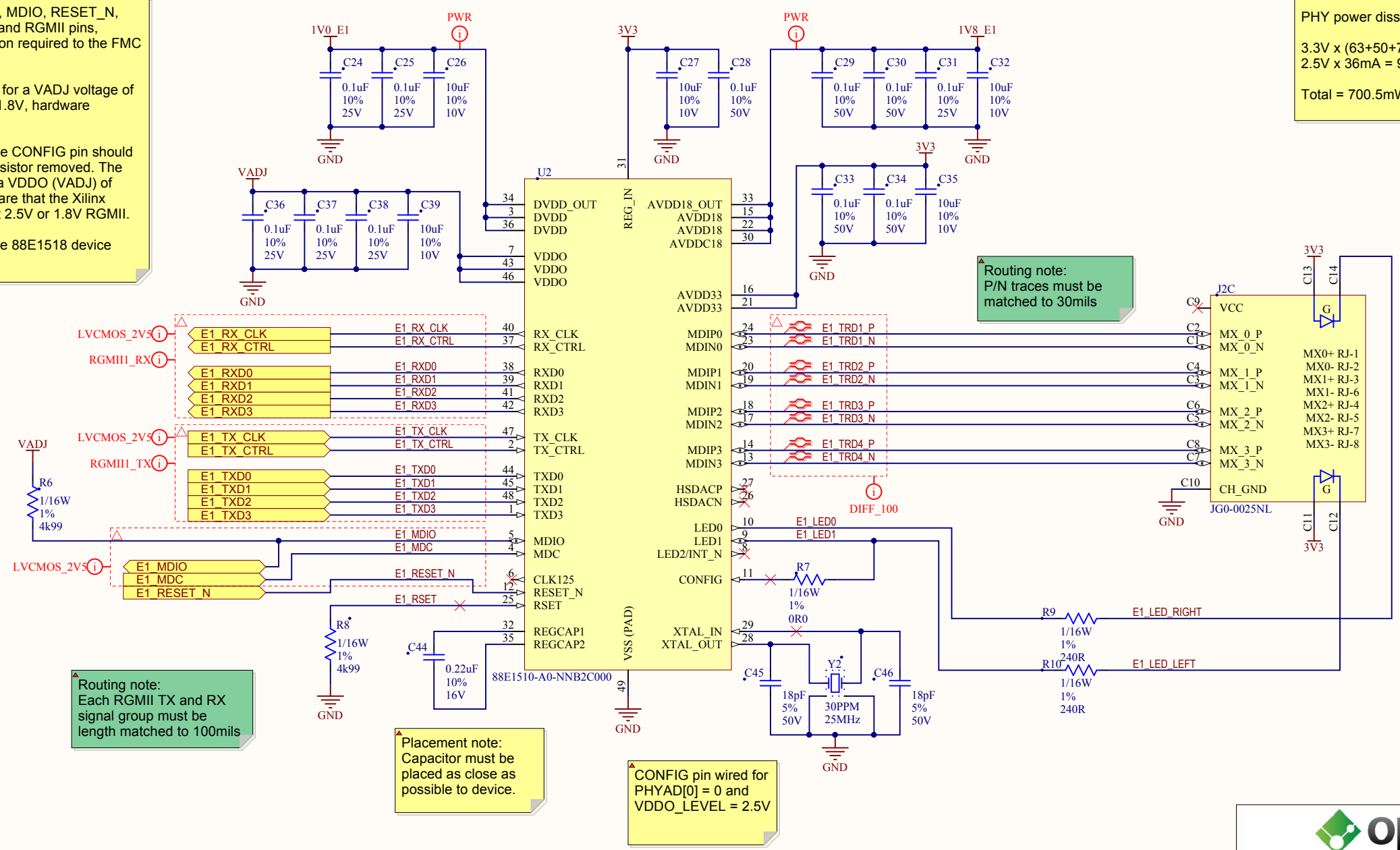
PHY current consumption:

1.8V supply: 63mA  
3.3V supply: 50mA  
1.0V supply: 72mA  
2.5V supply: 36mA

PHY power dissipated:

$3.3V \times (63+50+72mA) = 610.5mW$   
 $2.5V \times 36mA = 90mW$

Total = 700.5mW



Routing note:  
P/N traces must be matched to 30mils

Routing note:  
Each RGMII TX and RX signal group must be length matched to 100mils

Placement note:  
Capacitor must be placed as close as possible to device.

CONFIG pin wired for PHYAD[0] = 0 and VDDO\_LEVEL = 2.5V

**opsero**  
ELECTRONIC DESIGN

TITLE: Quad Gigabit Ethernet FMC

SHEET: Ethernet PHY 1

CONFIG: Standard

PROJECT: Quad Gigabit Ethernet FMC	DRAWN: J Johnson	DATE: 2014-09-11
SIZE: B	SCH P/N: OP031-01-SCH	REV. E.1 SHEET 4 OF 6

REV.	DESCRIPTION	DATE	APPROVED
E.1	Changed 125MHz oscillator to Micrel part FSEL option removed Added buffer to allow 1.8V CLK_EN	2016-02-06	J Johnson

VDDO (VADJ) supplies MDC, MDIO, RESET\_N, LED[2:0], CONFIG, CLK125 and RGMII pins, therefore no voltage conversion required to the FMC connector.

The standard configuration is for a VADJ voltage of 2.5V. For a VADJ of 3.3V or 1.8V, hardware modifications are required.

For VDDO (VADJ) of 3.3V, the CONFIG pin should be tied to GND and the OR resistor removed. The 88E1510 device will support a VDDO (VADJ) of 3.3V or 2.5V, however be aware that the Xilinx Series 7 devices only support 2.5V or 1.8V RGMII.

For VDDO (VADJ) of 1.8V, the 88E1518 device should be used.

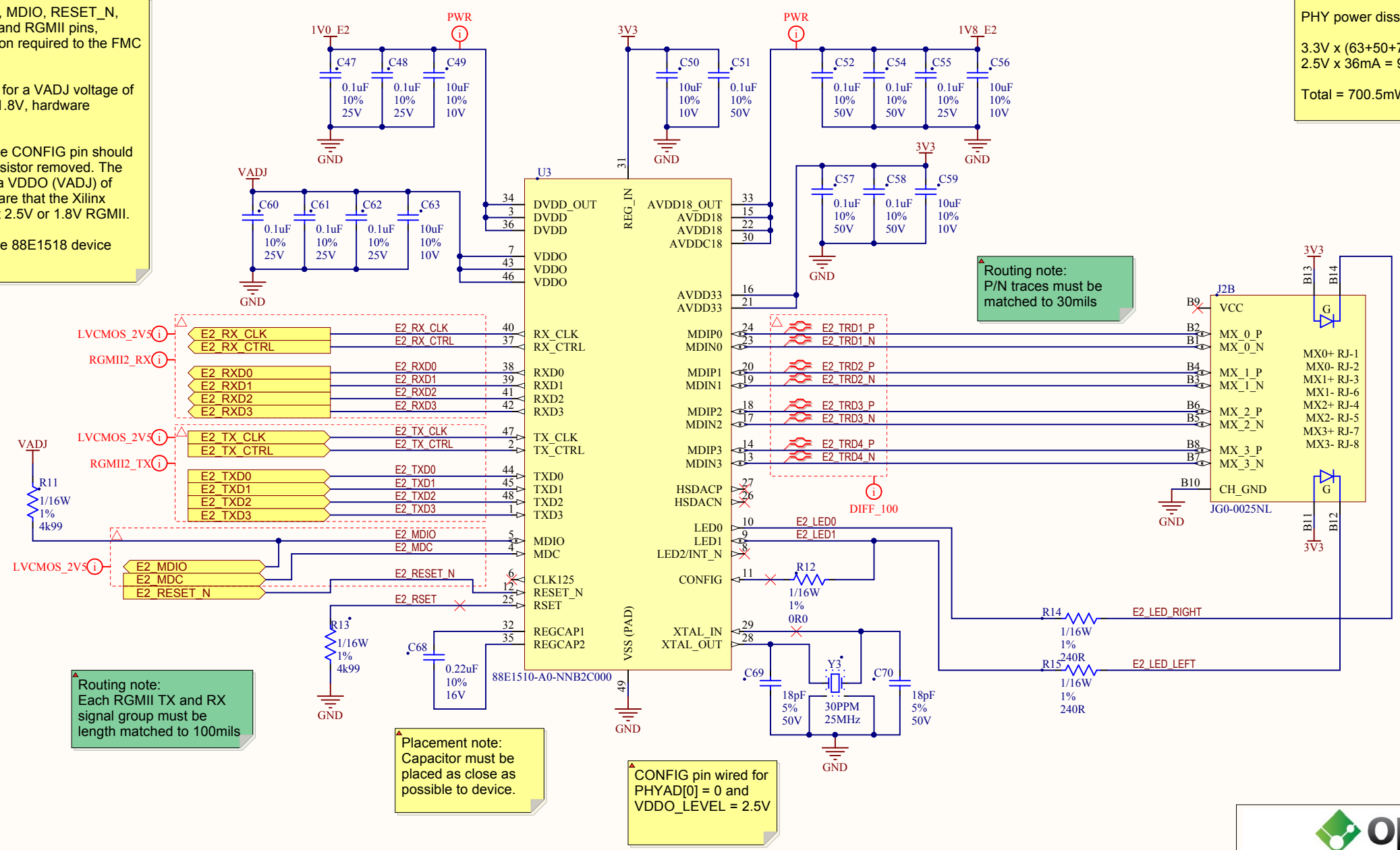
PHY current consumption:

1.8V supply: 63mA  
3.3V supply: 50mA  
1.0V supply: 72mA  
2.5V supply: 36mA

PHY power dissipated:

$3.3V \times (63+50+72mA) = 610.5mW$   
 $2.5V \times 36mA = 90mW$

Total = 700.5mW



Routing note:  
P/N traces must be matched to 30mils

Routing note:  
Each RGMII TX and RX signal group must be length matched to 100mils

Placement note:  
Capacitor must be placed as close as possible to device.

CONFIG pin wired for PHYAD[0] = 0 and VDDO\_LEVEL = 2.5V

TITLE Quad Gigabit Ethernet FMC			
SHEET Ethernet PHY 2			
CONFIG. Standard			
PROJECT	DRAWN	DATE	
Quad Gigabit Ethernet FMC	J Johnson	2014-09-11	
SIZE	SCH P/N.	REV.	SHEET OF
B	OP031-01-SCH	E.1	5 OF 6

REV.	DESCRIPTION	DATE	APPROVED
E.1	Changed 125MHz oscillator to Micrel part FSEL option removed Added buffer to allow 1.8V CLK_EN	2016-02-06	J Johnson

VDDO (VADJ) supplies MDC, MDIO, RESET\_N, LED[2:0], CONFIG, CLK125 and RGMII pins, therefore no voltage conversion required to the FMC connector.

The standard configuration is for a VADJ voltage of 2.5V. For a VADJ of 3.3V or 1.8V, hardware modifications are required.

For VDDO (VADJ) of 3.3V, the CONFIG pin should be tied to GND and the 0R resistor removed. The 88E1510 device will support a VDDO (VADJ) of 3.3V or 2.5V, however be aware that the Xilinx Series 7 devices only support 2.5V or 1.8V RGMII.

For VDDO (VADJ) of 1.8V, the 88E1518 device should be used.

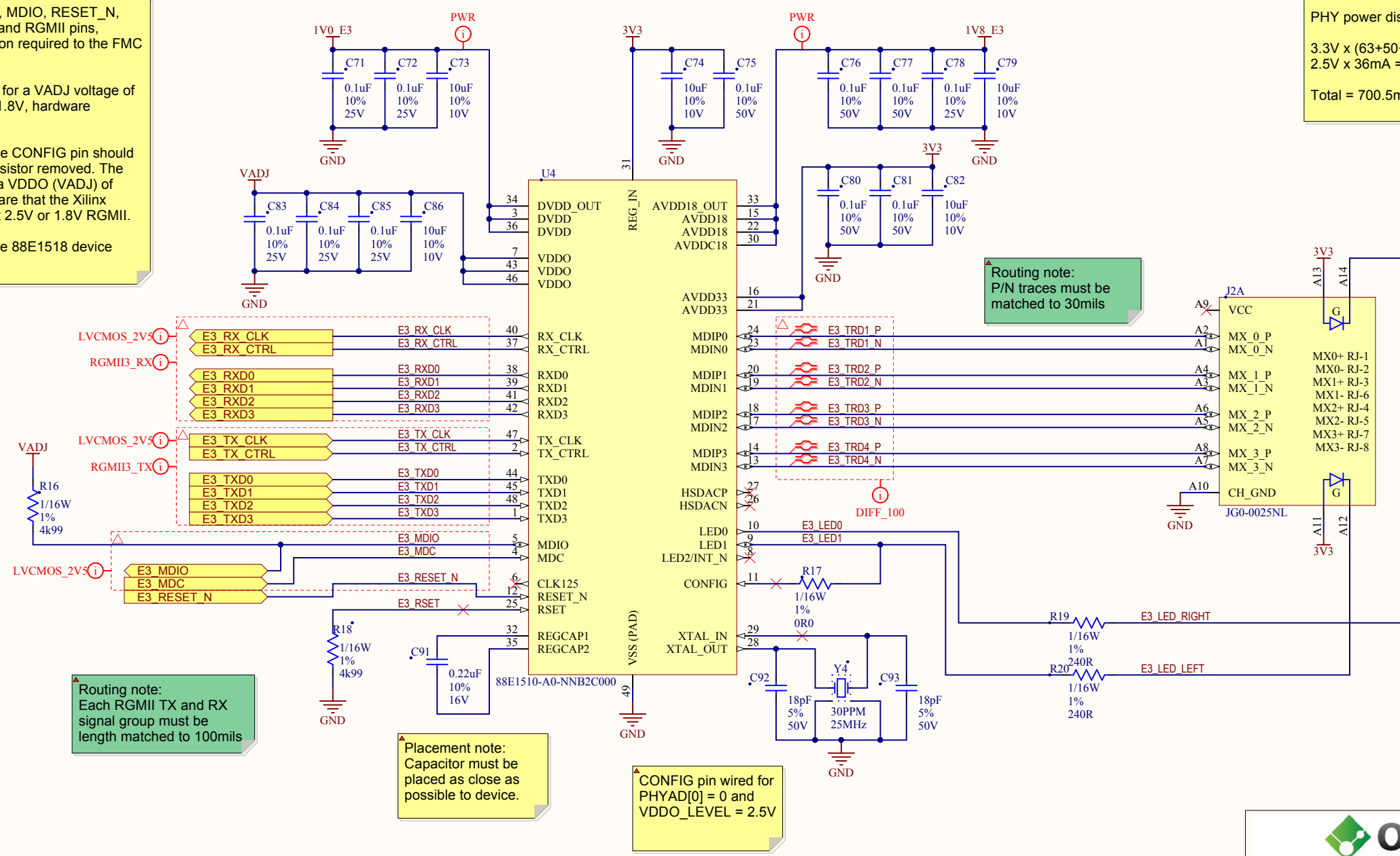
PHY current consumption:

1.8V supply: 63mA  
3.3V supply: 50mA  
1.0V supply: 72mA  
2.5V supply: 36mA

PHY power dissipated:

$3.3V \times (63+50+72mA) = 610.5mW$   
 $2.5V \times 36mA = 90mW$

Total = 700.5mW



Routing note:  
P/N traces must be matched to 30mils

Routing note:  
Each RGMII TX and RX signal group must be length matched to 100mils

Placement note:  
Capacitor must be placed as close as possible to device.

CONFIG pin wired for PHYAD[0] = 0 and VDDO\_LEVEL = 2.5V

TITLE Quad Gigabit Ethernet FMC			
SHEET Ethernet PHY 3			
CONFIG. Standard			
PROJECT	DRAWN	DATE	
Quad Gigabit Ethernet FMC	J Johnson	2014-09-11	
SIZE	SCH P/N.	REV.	SHEET OF
B	OP031-01-SCH	E.1	6 OF 6