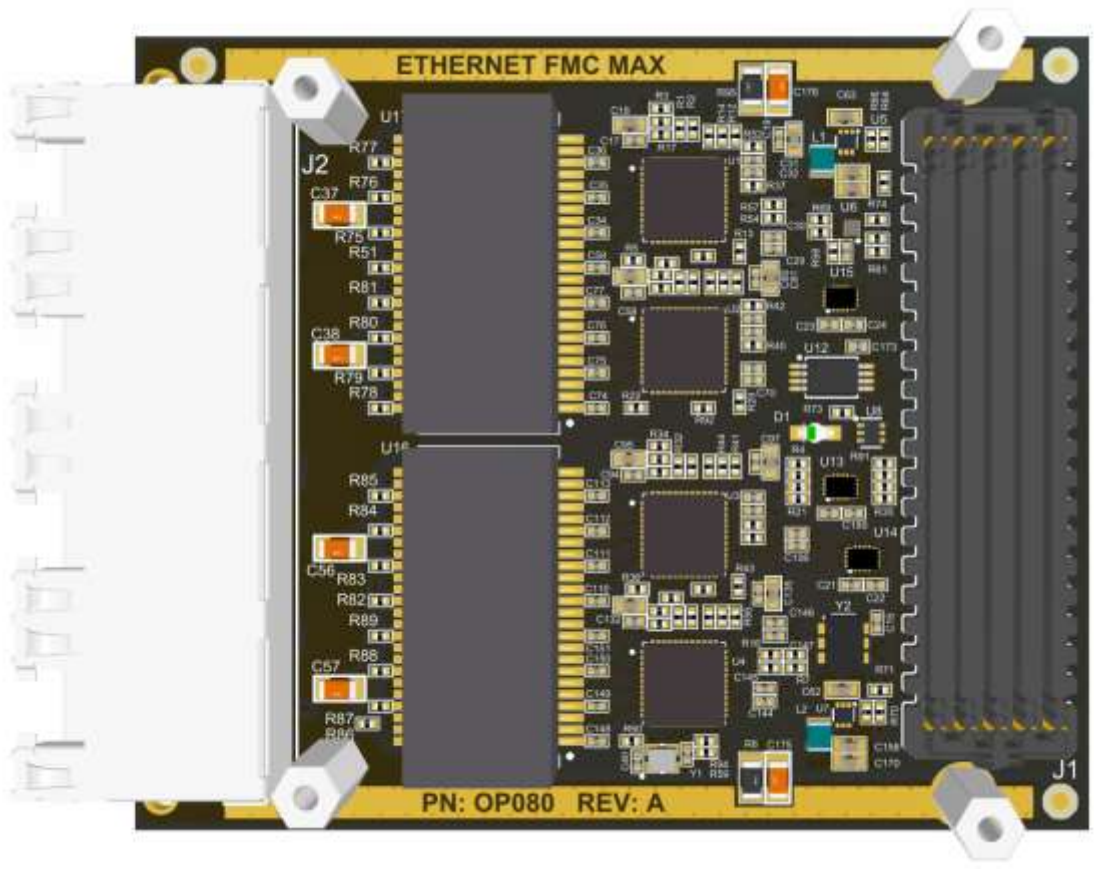
Ethernet FMC Max

Overview

Description

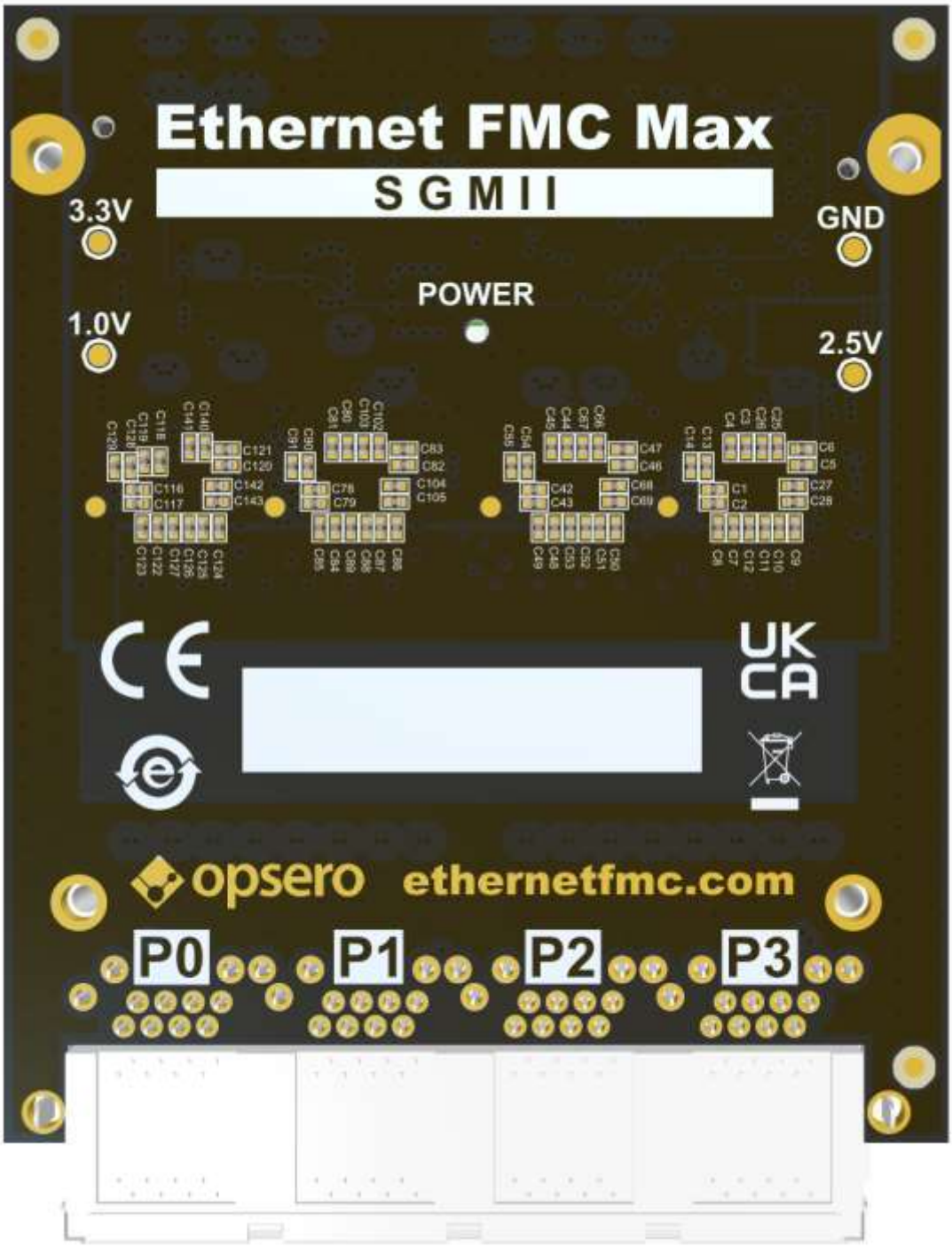
The Ethernet FMC Max is an add-on/expansion board (FPGA Mezzanine Card) for FPGA and SoC based development boards. The mezzanine card has 4x Texas Instruments DP83867 Gigabit Ethernet PHYs to provide 4 ports of gigabit Ethernet connectivity to the carrier development board.

Top view



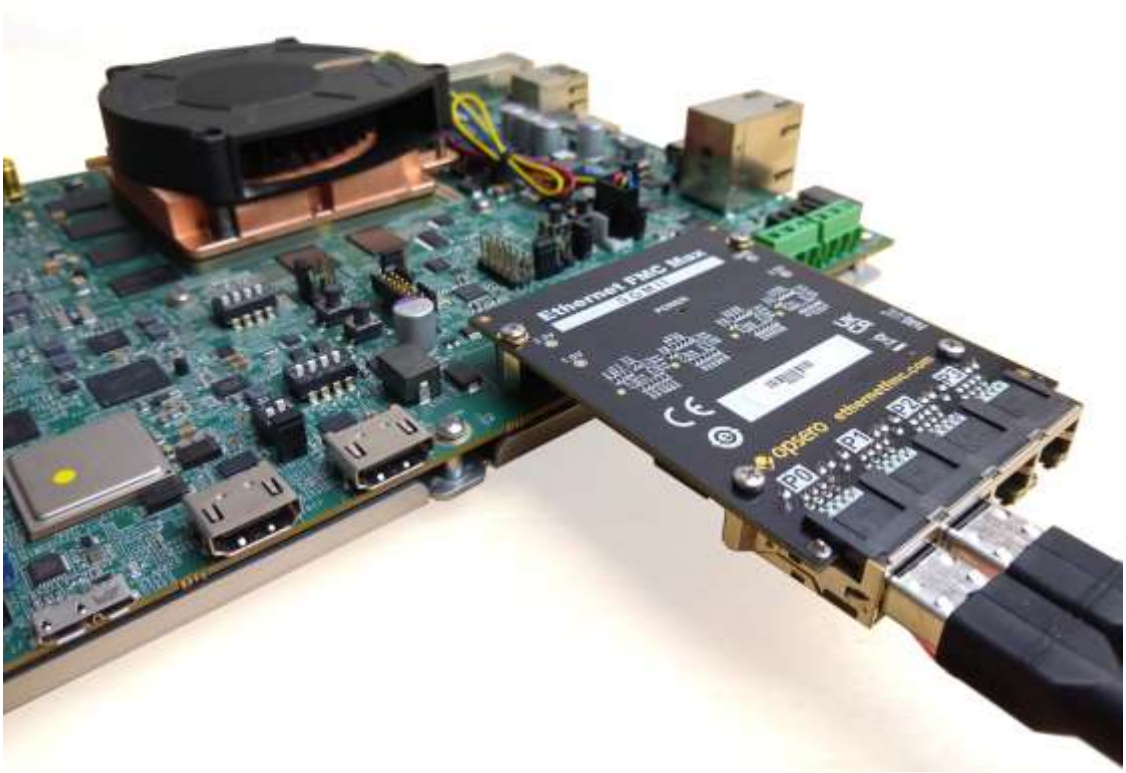
Ethernet FMC Max top

Bottom view



Ethernet FMC Max bottom

Application example



Ethernet FMC Max with VEK280

Features

- 4x Texas Instruments DP83867 Gigabit Ethernet PHYs
- Supports a wide range of I/O voltages (VADJ): 1.2V-2.5V
- High pin count FMC connector
- 4x SGMII PHY interfaces
- Quad Ethernet RJ45
- Discrete Ethernet magnetics
- FMC pinout conforms to VITA 57.1 FMC Standard
- Example designs with sources for several development boards
- Standalone and PetaLinux example designs

Ordering

The Ethernet FMC Max can be ordered from the vendors listed below. The links under the part number column will take you to the corresponding order page.

Vendor	Part name	Part number
Opsero	Ethernet FMC Max	OP080
Digi-Key	Ethernet FMC Max	OP080

Included with the Ethernet FMC Max are 2x machine screws for fixing the mezzanine card to the carrier board.

Pin Configuration

Pinout table

The Ethernet FMC Max has a high pin count FPGA Mezzanine Card (FMC) connector, providing the connections to the FPGA on the development board. The following table defines the pinout of the FMC connector and describes each pin's purpose on this mezzanine card.

Pin	Pin name	Net	Description
A1	GND	GND	Ground
A2	DP1_M2C_P	DP1_M2C_P	Port 1 PHY SGMII OUT positive
A3	DP1_M2C_N	DP1_M2C_N	Port 1 PHY SGMII OUT negative
A4	GND	GND	Ground
A5	GND	GND	Ground
A6	DP2_M2C_P	DP2_M2C_P	Port 2 PHY SGMII OUT positive
A7	DP2_M2C_N	DP2_M2C_N	Port 2 PHY SGMII OUT negative
A8	GND	GND	Ground
A9	GND	GND	Ground
A10	DP3_M2C_P	DP3_M2C_P	Port 3 PHY SGMII OUT positive
A11	DP3_M2C_N	DP3_M2C_N	Port 3 PHY SGMII OUT negative
A12	GND	GND	Ground
A13	GND	GND	Ground
A14	DP4_M2C_P	N/C	Not connected
A15	DP4_M2C_N	N/C	Not connected
A16	GND	GND	Ground
A17	GND	GND	Ground
A18	DP5_M2C_P	N/C	Not connected

A19	DP5_M2C_N	N/C	Not connected
A20	GND	GND	Ground
A21	GND	GND	Ground
A22	DP1_C2M_P	DP1_C2M_P	Port 1 PHY SGMII IN positive
A23	DP1_C2M_N	DP1_C2M_N	Port 1 PHY SGMII IN negative
A24	GND	GND	Ground
A25	GND	GND	Ground
A26	DP2_C2M_P	DP2_C2M_P	Port 2 PHY SGMII IN positive
A27	DP2_C2M_N	DP2_C2M_N	Port 2 PHY SGMII IN negative
A28	GND	GND	Ground
A29	GND	GND	Ground
A30	DP3_C2M_P	DP3_C2M_P	Port 3 PHY SGMII IN positive
A31	DP3_C2M_N	DP3_C2M_N	Port 3 PHY SGMII IN negative
A32	GND	GND	Ground
A33	GND	GND	Ground
A34	DP4_C2M_P	N/C	Not connected
A35	DP4_C2M_N	N/C	Not connected
A36	GND	GND	Ground
A37	GND	GND	Ground
A38	DP5_C2M_P	N/C	Not connected
A39	DP5_C2M_N	N/C	Not connected
A40	GND	GND	Ground
B1	CLK_DIR	N/C	Not connected
B2	GND	GND	Ground

B3	GND	GND	Ground
B4	DP9_M2C_P	N/C	Not connected
B5	DP9_M2C_N	N/C	Not connected
B6	GND	GND	Ground
B7	GND	GND	Ground
B8	DP8_M2C_P	N/C	Not connected
B9	DP8_M2C_N	N/C	Not connected
B10	GND	GND	Ground
B11	GND	GND	Ground
B12	DP7_M2C_P	N/C	Not connected
B13	DP7_M2C_N	N/C	Not connected
B14	GND	GND	Ground
B15	GND	GND	Ground
B16	DP6_M2C_P	N/C	Not connected
B17	DP6_M2C_N	N/C	Not connected
B18	GND	GND	Ground
B19	GND	GND	Ground
B20	GBTCLK1_M2C_P	N/C	Not connected
B21	GBTCLK1_M2C_N	N/C	Not connected
B22	GND	GND	Ground
B23	GND	GND	Ground
B24	DP9_C2M_P	N/C	Not connected
B25	DP9_C2M_N	N/C	Not connected
B26	GND	GND	Ground

B27	GND	GND	Ground
B28	DP8_C2M_P	N/C	Not connected
B29	DP8_C2M_N	N/C	Not connected
B30	GND	GND	Ground
B31	GND	GND	Ground
B32	DP7_C2M_P	N/C	Not connected
B33	DP7_C2M_N	N/C	Not connected
B34	GND	GND	Ground
B35	GND	GND	Ground
B36	DP6_C2M_P	N/C	Not connected
B37	DP6_C2M_N	N/C	Not connected
B38	GND	GND	Ground
B39	GND	GND	Ground
B40	RES0	N/C	Not connected
C1	GND	GND	Ground
C2	DP0_C2M_P	DP0_C2M_P	Port 0 PHY SGMII IN positive
C3	DP0_C2M_N	DP0_C2M_N	Port 0 PHY SGMII IN negative
C4	GND	GND	Ground
C5	GND	GND	Ground
C6	DP0_M2C_P	DP0_M2C_P	Port 0 PHY SGMII OUT positive
C7	DP0_M2C_N	DP0_M2C_N	Port 0 PHY SGMII OUT negative
C8	GND	GND	Ground
C9	GND	GND	Ground
C10	LA06_P	N/C	Not connected

C11	LA06_N	N/C	Not connected
C12	GND	GND	Ground
C13	GND	GND	Ground
C14	LA10_P	N/C	Not connected
C15	LA10_N	N/C	Not connected
C16	GND	GND	Ground
C17	GND	GND	Ground
C18	LA14_P	N/C	Not connected
C19	LA14_N	N/C	Not connected
C20	GND	GND	Ground
C21	GND	GND	Ground
C22	LA18_P_CC	N/C	Not connected
C23	LA18_N_CC	N/C	Not connected
C24	GND	GND	Ground
C25	GND	GND	Ground
C26	LA27_P	N/C	Not connected
C27	LA27_N	N/C	Not connected
C28	GND	GND	Ground
C29	GND	GND	Ground
C30	SCL	I2C_SCL	I2C Clock
C31	SDA	I2C_SDA	I2C Data (bidirectional)
C32	GND	GND	Ground
C33	GND	GND	Ground
C34	GA0	GA0	EEPROM Address Bit 1 (A1)

C35	12P0V_1	12V0	12VDC
C36	GND	GND	Ground
C37	12P0V_2	12V0	12VDC
C38	GND	GND	Ground
C39	3P3V_1	3V3	Not connected
C40	GND	GND	Ground
D1	PG_C2M	PG	Power Good (Driven by carrier)
D2	GND	GND	Ground
D3	GND	GND	Ground
D4	GBTCLK0_M2C_P	GBTCLK0_M2C_P	125MHz Ethernet reference clock for the FPGA
D5	GBTCLK0_M2C_N	GBTCLK0_M2C_N	125MHz Ethernet reference clock for the FPGA
D6	GND	GND	Ground
D7	GND	GND	Ground
D8	LA01_P_CC	N/C	Not connected
D9	LA01_N_CC	N/C	Not connected
D10	GND	GND	Ground
D11	LA05_P	N/C	Not connected
D12	LA05_N	N/C	Not connected
D13	GND	GND	Ground
D14	LA09_P	N/C	Not connected
D15	LA09_N	N/C	Not connected
D16	GND	GND	Ground
D17	LA13_P	PG_1V0	Power good signal from 1.0V buck converter

D18	LA13_N	PG_2V5	Power good signal from 2.5V buck converter
D19	GND	GND	Ground
D20	LA17_P_CC	MDC_T	MDIO bus clock (FPGA to PHY)
D21	LA17_N_CC	MDIO_T	MDIO bus data (bidirectional)
D22	GND	GND	Ground
D23	LA23_P	N/C	Not connected
D24	LA23_N	N/C	Not connected
D25	GND	GND	Ground
D26	LA26_P	N/C	Not connected
D27	LA26_N	N/C	Not connected
D28	GND	GND	Ground
D29	TCK	N/C	Not connected
D30	TDI	TDI	Connects to TDO to close JTAG chain
D31	TDO	TDO	Connects to TDI to close JTAG chain
D32	3P3VAUX	3V3AUX	3.3VDC Power supply for EEPROM
D33	TMS	N/C	Not connected
D34	TRST_L	N/C	Not connected
D35	GA1	GA1	EEPROM Address Bit 0 (A0)
D36	3P3V_2	3V3	3.3VDC main FMC power supply
D37	GND	GND	Ground
D38	3P3V_3	3V3	3.3VDC main FMC power supply
D39	GND	GND	Ground
D40	3P3V_4	3V3	3.3VDC main FMC power supply

E1	GND	GND	Ground
E2	HA01_P_CC	N/C	Not connected
E3	HA01_N_CC	N/C	Not connected
E4	GND	GND	Ground
E5	GND	GND	Ground
E6	HA05_P	N/C	Not connected
E7	HA05_P	N/C	Not connected
E8	GND	GND	Ground
E9	HA09_P	N/C	Not connected
E10	HA09_P	N/C	Not connected
E11	GND	GND	Ground
E12	HA13_P	N/C	Not connected
E13	HA13_P	N/C	Not connected
E14	GND	GND	Ground
E15	HA16_P	N/C	Not connected
E16	HA16_P	N/C	Not connected
E17	GND	GND	Ground
E18	HA20_P	N/C	Not connected
E19	HA20_P	N/C	Not connected
E20	GND	GND	Ground
E21	HB03_P	N/C	Not connected
E22	HB03_P	N/C	Not connected
E23	GND	GND	Ground
E24	HB05_P	N/C	Not connected

E25	HB05_P	N/C	Not connected
E26	GND	GND	Ground
E27	HB09_P	N/C	Not connected
E28	HB09_P	N/C	Not connected
E29	GND	GND	Ground
E30	HB13_P	N/C	Not connected
E31	HB13_P	N/C	Not connected
E32	GND	GND	Ground
E33	HB19_P	N/C	Not connected
E34	HB19_P	N/C	Not connected
E35	GND	GND	Ground
E36	HB21_P	N/C	Not connected
E37	HB21_P	N/C	Not connected
E38	GND	GND	Ground
E39	VADJ_1	N/C	Adjustable IO power supply voltage
E40	GND	GND	Ground
F1	PG_M2C	N/C	Not connected
F2	GND	GND	Ground
F3	GND	GND	Ground
F4	HA00_P_CC	N/C	Not connected
F5	HA00_P_CC	N/C	Not connected
F6	GND	GND	Ground
F7	HA04_P	N/C	Not connected
F8	HA04_P	N/C	Not connected

F9	GND	GND	Ground
F10	HA08_P	N/C	Not connected
F11	HA08_P	N/C	Not connected
F12	GND	GND	Ground
F13	HA12_P	N/C	Not connected
F14	HA12_P	N/C	Not connected
F15	GND	GND	Ground
F16	HA15_P	N/C	Not connected
F17	HA15_P	N/C	Not connected
F18	GND	GND	Ground
F19	HA19_P	N/C	Not connected
F20	HA19_P	N/C	Not connected
F21	GND	GND	Ground
F22	HB02_P	N/C	Not connected
F23	HB02_P	N/C	Not connected
F24	GND	GND	Ground
F25	HB04_P	N/C	Not connected
F26	HB04_P	N/C	Not connected
F27	GND	GND	Ground
F28	HB08_P	N/C	Not connected
F29	HB08_P	N/C	Not connected
F30	GND	GND	Ground
F31	HB12_P	N/C	Not connected
F32	HB12_P	N/C	Not connected

F33	GND	GND	Ground
F34	HB16_P	N/C	Not connected
F35	HB16_P	N/C	Not connected
F36	GND	GND	Ground
F37	HB20_P	N/C	Not connected
F38	HB20_P	N/C	Not connected
F39	GND	GND	Ground
F40	VADJ_2	N/C	Adjustable IO power supply voltage
J1	GND	GND	Ground
J2	CLK3_BIDIR_P	N/C	Not connected
J3	CLK3_BIDIR_P	N/C	Not connected
J4	GND	GND	Ground
J5	GND	GND	Ground
J6	HA03_P	N/C	Not connected
J7	HA03_P	N/C	Not connected
J8	GND	GND	Ground
J9	HA07_P	N/C	Not connected
J10	HA07_P	N/C	Not connected
J11	GND	GND	Ground
J12	HA11_P	N/C	Not connected
J13	HA11_P	N/C	Not connected
J14	GND	GND	Ground
J15	HA14_P	N/C	Not connected
J16	HA14_P	N/C	Not connected

J17	GND	GND	Ground
J18	HA18_P	N/C	Not connected
J19	HA18_P	N/C	Not connected
J20	GND	GND	Ground
J21	HA22_P	N/C	Not connected
J22	HA22_P	N/C	Not connected
J23	GND	GND	Ground
J24	HB01_P	N/C	Not connected
J25	HB01_P	N/C	Not connected
J26	GND	GND	Ground
J27	HB07_P	N/C	Not connected
J28	HB07_P	N/C	Not connected
J29	GND	GND	Ground
J30	HB11_P	N/C	Not connected
J31	HB11_P	N/C	Not connected
J32	GND	GND	Ground
J33	HB15_P	N/C	Not connected
J34	HB15_P	N/C	Not connected
J35	GND	GND	Ground
J36	HB18_P	N/C	Not connected
J37	HB18_P	N/C	Not connected
J38	GND	GND	Ground
J39	VIO_B_M2C_1	N/C	Not connected
J40	GND	GND	Ground

K1	VREF_B_M2C	N/C	Not connected
K2	GND	GND	Ground
K3	GND	GND	Ground
K4	CLK2_BIDIR_P	N/C	Not connected
K5	CLK2_BIDIR_P	N/C	Not connected
K6	GND	GND	Ground
K7	HA02_P	N/C	Not connected
K8	HA02_P	N/C	Not connected
K9	GND	GND	Ground
K10	HA06_P	N/C	Not connected
K11	HA06_P	N/C	Not connected
K12	GND	GND	Ground
K13	HA10_P	N/C	Not connected
K14	HA10_P	N/C	Not connected
K15	GND	GND	Ground
K16	HA17_P_CC	N/C	Not connected
K17	HA17_P_CC	N/C	Not connected
K18	GND	GND	Ground
K19	HA21_P	N/C	Not connected
K20	HA21_P	N/C	Not connected
K21	GND	GND	Ground
K22	HA23_P	N/C	Not connected
K23	HA23_P	N/C	Not connected
K24	GND	GND	Ground

K25	HB00_P_CC	N/C	Not connected
K26	HB00_P_CC	N/C	Not connected
K27	GND	GND	Ground
K28	HB06_P_CC	N/C	Not connected
K29	HB06_P_CC	N/C	Not connected
K30	GND	GND	Ground
K31	HB10_P	N/C	Not connected
K32	HB10_P	N/C	Not connected
K33	GND	GND	Ground
K34	HB14_P	N/C	Not connected
K35	HB14_P	N/C	Not connected
K36	GND	GND	Ground
K37	HB17_P_CC	N/C	Not connected
K38	HB17_P_CC	N/C	Not connected
K39	GND	GND	Ground
K40	VIO_B_M2C_2	N/C	Not connected
G1	GND	GND	Ground
G2	CLK1_M2C_P	N/C	Not connected
G3	CLK1_M2C_N	N/C	Not connected
G4	GND	GND	Ground
G5	GND	GND	Ground
G6	LA00_P_CC	N/C	Not connected
G7	LA00_N_CC	N/C	Not connected
G8	GND	GND	Ground

G9	LA03_P	N/C	Not connected
G10	LA03_N	N/C	Not connected
G11	GND	GND	Ground
G12	LA08_P	E0_GPIO0_T	Port 0 PHY GPIO0 output
G13	LA08_N	E0_GPIO1_T	Port 0 PHY GPIO1 output
G14	GND	GND	Ground
G15	LA12_P	E0_RESET_N_T	Port 0 PHY reset input (active low)
G16	LA12_N	E1_RESET_N_T	Port 1 PHY reset input (active low)
G17	GND	GND	Ground
G18	LA16_P	E2_GPIO0_T	Port 2 PHY GPIO0 output
G19	LA16_N	E2_GPIO1_T	Port 2 PHY GPIO1 output
G20	GND	GND	Ground
G21	LA20_P	N/C	Not connected
G22	LA20_N	N/C	Not connected
G23	GND	GND	Ground
G24	LA22_P	N/C	Not connected
G25	LA22_N	N/C	Not connected
G26	GND	GND	Ground
G27	LA25_P	N/C	Not connected
G28	LA25_N	N/C	Not connected
G29	GND	GND	Ground
G30	LA29_P	N/C	Not connected
G31	LA29_N	N/C	Not connected
G32	GND	GND	Ground

G33	LA31_P	N/C	Not connected
G34	LA31_N	N/C	Not connected
G35	GND	GND	Ground
G36	LA33_P	N/C	Not connected
G37	LA33_N	N/C	Not connected
G38	GND	GND	Ground
G39	VADJ_3	VADJ	Adjustable IO power supply voltage
G40	GND	GND	Ground
H1	VREF_A_M2C	N/C	Not connected
H2	PRSNT_M2C_L	GND	Ground
H3	GND	GND	Ground
H4	CLK0_M2C_P	N/C	Not connected
H5	CLK0_M2C_N	N/C	Not connected
H6	GND	GND	Ground
H7	LA02_P	N/C	Not connected
H8	LA02_N	N/C	Not connected
H9	GND	GND	Ground
H10	LA04_P	N/C	Not connected
H11	LA04_N	N/C	Not connected
H12	GND	GND	Ground
H13	LA07_P	E1_GPIO0_T	Port 1 PHY GPIO0 output
H14	LA07_N	E1_GPIO1_T	Port 1 PHY GPIO1 output
H15	GND	GND	Ground
H16	LA11_P	E2_RESET_N_T	Port 2 PHY reset input (active low)

H17	LA11_N	E3_RESET_N_T	Port 3 PHY reset input (active low)
H18	GND	GND	Ground
H19	LA15_P	E3_GPIO0_T	Port 3 PHY GPIO0 output
H20	LA15_N	E3_GPIO1_T	Port 3 PHY GPIO1 output
H21	GND	GND	Ground
H22	LA19_P	N/C	Not connected
H23	LA19_N	N/C	Not connected
H24	GND	GND	Ground
H25	LA21_P	N/C	Not connected
H26	LA21_N	N/C	Not connected
H27	GND	GND	Ground
H28	LA24_P	N/C	Not connected
H29	LA24_N	N/C	Not connected
H30	GND	GND	Ground
H31	LA28_P	N/C	Not connected
H32	LA28_N	N/C	Not connected
H33	GND	GND	Ground
H34	LA30_P	N/C	Not connected
H35	LA30_N	N/C	Not connected
H36	GND	GND	Ground
H37	LA32_P	N/C	Not connected
H38	LA32_N	N/C	Not connected
H39	GND	GND	Ground
H40	VADJ_4	VADJ	Adjustable IO power supply voltage

Specifications

Recommended Operating Conditions

SUPPLY VOLTAGE	MIN	TYP	MAX	UNIT
12 VDC	+11.4	+12	+12.6	V
3.3 VDC	+3.14	+3.3	+3.46	V
VADJ (1.2VDC)	+1.14	+1.2	+1.26	V
VADJ (1.5VDC)	+1.425	+1.5	+1.575	V
VADJ (1.8VDC)	+1.71	+1.8	+1.89	V
VADJ (2.5VDC)	+2.375	+2.5	+2.625	V

Notes: * All VADJ pins must be supplied with the same voltage chosen from one of the following levels: +1.2VDC, +1.5VDC, +1.8VDC, +2.5VDC. Note that many carriers have a system controller that will make this choice for you.

Power Consumption

Power consumption measurements will be added to this section in the near future.

Thermal Information

We have not performed comprehensive thermal testing on the Ethernet FMC Max, however we recommend that it be operated under ambient temperatures between -40 and 85 degrees C. This advice is based on the recommended ambient operating temperatures of the critical devices on the Ethernet FMC Max. These temperatures are listed in the table below.

DEVICE	MIN	MAX	UNIT
TI, 1A Step Down Converter, TLV62568APDRLR	-40	125	C
TI, 10/100/1000 Ethernet PHY, DP83867ISRGZ	-40	85	C
Link-PP, Quad RJ45, LPJE4718AGNL	-40	85	C
Skyworks, Crystal Oscillator 125MHz, 511BBA125M000BAG	-40	85	C

ON Semi, TinyLogic ULP-A Dual Buffer, NC7WV16P6X	-40	85	C
Link-PP, Quad Ethernet Magnetics, LP84862ANL	-40	85	C
TI, Voltage Translator, SN74AVC4T245RSVR	-40	85	C

Components that are not listed in the table above (such as resistors, capacitors) are selected to have minimum operating temperature that is lower than -40 degrees C, and maximum operating temperature that is greater than 85 degrees C.

Reset Timing

When hardware resetting the PHYs, we recommend using this timing:

1. Hold the RESET_N signal LOW for 1ms
2. Release the RESET_N signal (HIGH) and wait for 1ms

I2C (EEPROM) Timing

The serial EEPROM (part number ST, 2K EEPROM, M24C02-FDW6TP) has a maximum operating clock frequency of 400 kHz.

MDIO Timing

- The maximum MDC frequency supported by the DP83867 PHY is 25MHz.

DP83867 Electrical and Timing

For electrical specs and timing related to the DP83867 signals listed below, please refer to the DP83867 datasheet:

- Reset
- SGMII
- MDIO

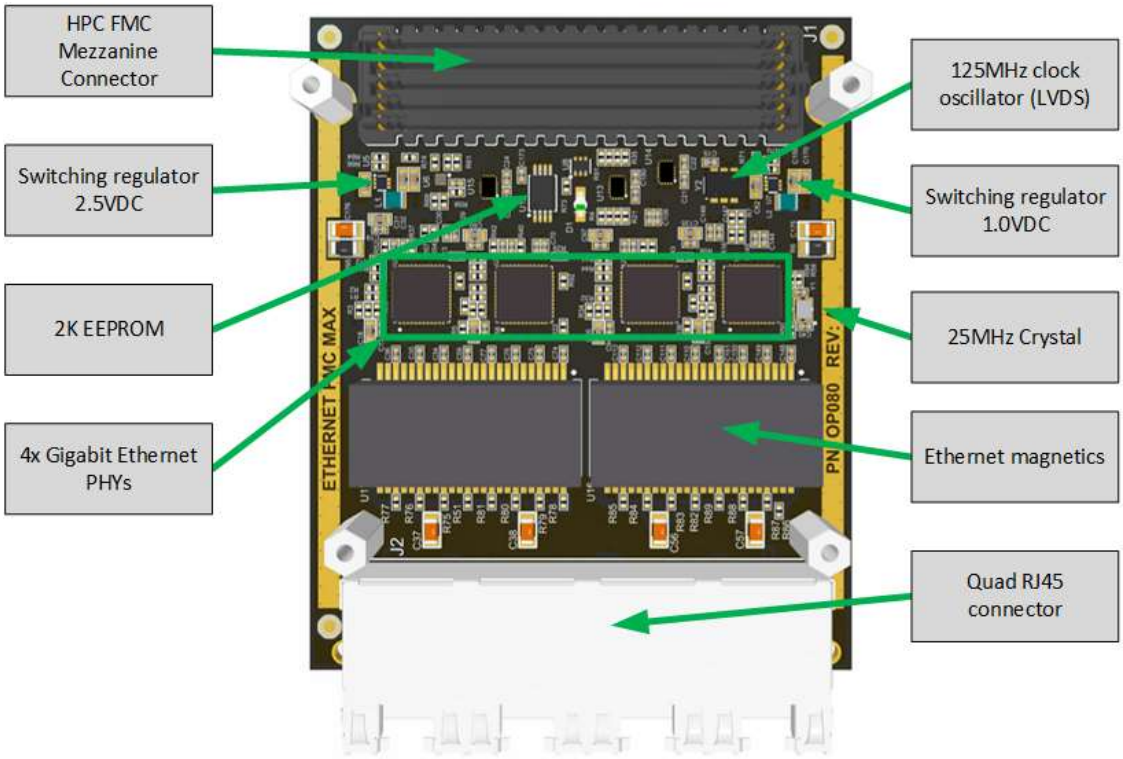
Certifications

- RoHS
- CE

Detailed Description

Hardware Overview

The figure below illustrates the various hardware components that are located on the top-side (component side) of the Ethernet FMC Max.

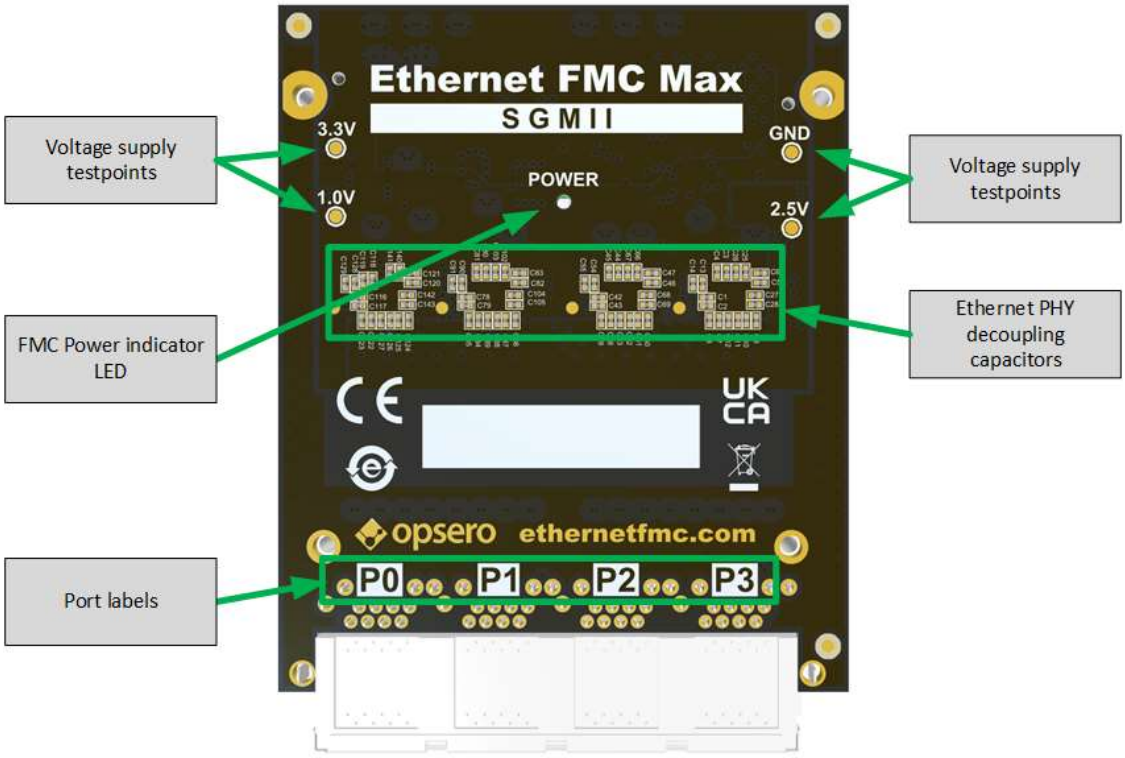


{#ethernet-fmc-max-top-labelled}

The main components on the top-side of the mezzanine card are:

- 4x TI DP83867 Gigabit Ethernet PHYs
- High Pin Count FMC Connector
- 2K EEPROM
- 125MHz Clock Oscillator
- 25MHz crystal
- Ethernet magnetics
- Quad RJ45 connector
- Switching regulators (1.0V and 2.5V)
- Voltage translators

The figure below illustrates the various hardware components that are located on the bottom-side of the mezzanine card.



{#ethernet-fmc-max-bottom-labelled}

The main components on the bottom-side of the mezzanine card are:

- Decoupling capacitors for the TI DP83867 Gigabit Ethernet PHYs
- Power indicator LED
- Test points for power supplies
- Port labels (P0,P1,P2,P3)

TI DP83867 Gigabit Ethernet PHY

There are 4x TI DP83867 Gigabit Ethernet PHYs on the mezzanine card, one for each of the four Gigabit Ethernet ports. For interfacing with a MAC, the DP83867 has an SGMII (Serial GMII) interface. The DP83867 is designed for low-power, low-latency and features Time Sensitive Network (TSN) compliance, IEEE 1588 Start of Frame Detection and Wake-on-LAN packet detection. For more specific information on the DP83867, please refer to the DP83867 datasheet.

In this documentation, we will refer to the ports and respective PHYs as P0, P1, P2 and P3, corresponding to their placement from left-to-right and as shown in Ethernet FMC Max bottom labelled image.

Strap Configuration

Certain PHY settings are hard wired by resistors connected to “strap” pins of the DP83867 device. These pins determine the value of these settings on power-up of the device, however they can be changed by software by writing to the appropriate PHY registers via the MDIO bus.

The table below describes the strap configuration of the Ethernet FMC Max.

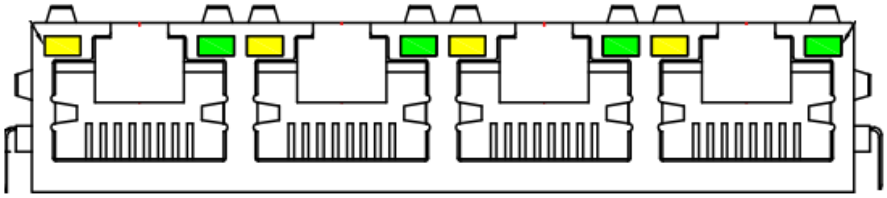
Strap Pin	Strap Mode	Strap Function
RX_D0	2 (P0) 4 (P1) 1 (P2) 4 (P3)	PHY address [1:0] = 01 PHY address [1:0] = 11 PHY address [1:0] = 00 PHY address [1:0] = 11
RX_D2	1 (P0) 1 (P1) 4 (P2) 4 (P3)	PHY address [3:2] = 00 PHY address [3:2] = 00 PHY address [3:2] = 11 PHY address [3:2] = 11
RX_CTRL	3	Auto-Negotiation Enable
GPIO_0	1	N/A
GPIO_1	1	N/A
LED_2	1	N/A
LED_1	1	Advertise Ability of 10/100/1000
LED_0	2 (Rev-A) 4 (Rev-B and up)	Mirror Enable = 0, SGMII Enable = 1 Mirror Enable = 1, SGMII Enable = 1

Notes: * Straps RX_D0 and RX_D2 determine the PHY addresses that are used to target each PHY for MDIO read and writes. More information about configuring the PHYs via MDIO can be found in the MDIO section. * Straps GPIO_0, GPIO_1 and LED_2 pertain to PHY settings related to the RGMII interface and are not relevant to the Ethernet FMC Max. * The LED_0 strap on Rev-A boards (serial numbers 800000-800019) is set to mode 2 which disables Mirror Mode. For correct operation of the Ethernet ports on Rev-A boards, the Mirror Mode setting must be enabled by software (write 0x1 to bit 0 of CFG4 register address 0x0031). The software for this is integrated

into our reference designs; you should only need to handle this when writing custom software.

RJ45 Connector and magnetics

The Ethernet FMC Max uses a quad RJ45 connector (Link-PP, Quad RJ45, LPJE4718AGNL) and discrete Ethernet magnetics (Link-PP, Quad Ethernet Magnetics, LP84862ANL).



Ethernet FMC Max RJ45 LEDs

As illustrated by the image above, each port on the RJ45 connector has two LEDs, one green and one yellow. The green LED is on the right side of the port (when the tab is pointed up), while the yellow LED is on the left side. The LEDs are connected to the DP83867 PHY as shown in the table below:

Color	Side	PHY connection	Default operation mode
Green	Right	LED_1	1G link established
Yellow	Left	LED_0	Link established

The operation mode of these LEDs can be changed by writing to the LED Configuration Register (LEDCR1, Address 0x0018) of the TI DP83867 PHY. Refer to the datasheet for more information.

EEPROM

The 2K EEPROM stores IPMI FRU data that can be read by the carrier board and contains the following information:

- Manufacturer name (Opsero Electronic Design Inc.)
- Product name
- Product part number
- Serial number
- Power supply requirements

The FRU data is read by some carrier boards to determine the correct VADJ voltage to apply to the mezzanine card. All Opsero FMC products have their EEPROMs programmed with valid FRU data to allow these carrier boards to correctly power them.

Erasing or writing over the contents of the EEPROM can corrupt the IPMI FRU data making the mezzanine card unusable with carrier boards that require the information. We recommend that you do not use the mezzanine card's EEPROM for non-volatile storage but instead use the storage options provided by the carrier board. If you mistakenly erase or corrupt the contents of the EEPROM, you can reprogram it using the Opsero FMC EEPROM Tool. Read more about the FMC EEPROM tool in the User Guide.

High Pin Count FMC Connector

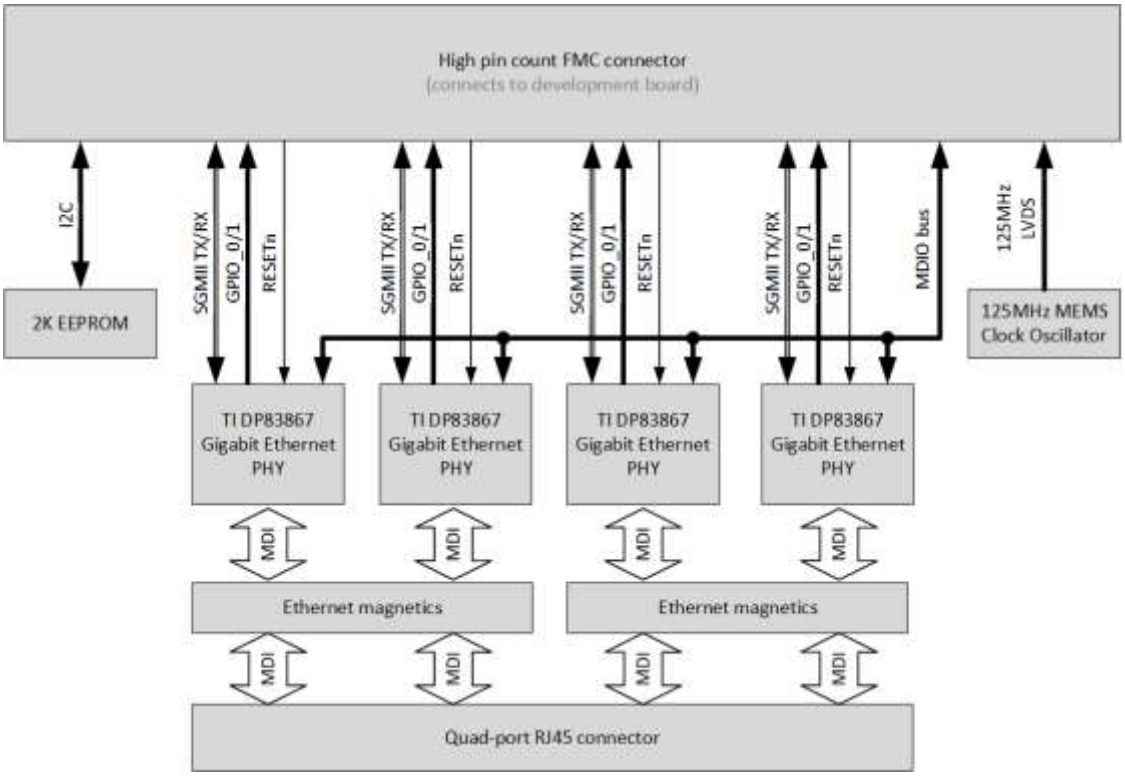
The Ethernet FMC Max has a high pin count FMC (FPGA Mezzanine Card) connector for interfacing with an FPGA or SoC development board. The part number of this connector is Samtec, Mezzanine-side High pin count FMC Connector, ASP-134488-01 . The pinout of this connector conforms to the VITA 57.1 FPGA Mezzanine Card Standard (for more information, see Pin configuration. For more information on the FMC connector and the VITA 57.1 standard, see the Samtec page on VITA 57.1 .

I/O Interfaces

The FMC connector provides power to the Ethernet FMC and also presents the following I/O signals to the FPGA fabric of the development board:

- SGMII (gigabit transceivers) for each of the PHYs
- Reset signal (active low) for each of the PHYs
- Single MDIO bus shared by all PHYs
- GPIO_0 and GPIO_1 PHY outputs
- I2C for EEPROM R/W access
- 125MHz LVDS clock
- Power good signals from the buck converters (PG_1V0 and PG_2V5, left out of the figure for simplicity)

The figure below illustrates the connections to the FMC connector.



{#ethernet-fmc-max-fmc}

Note that the level translators are left out of the diagram for simplicity.

Level translation

To support a wide range of I/O voltages (VADJ), the Ethernet FMC Max uses level translators for the MDIO bus, the PHY reset signals and the PHY GPIO_0/1 signals. The table below lists the devices used:

Device	Purpose
LSF0102DQER	Level translation of the shared PHY MDIO bus.
SN74AVC4T245RSVR	Level translation of PHY resets and GPIO_0/1.

The other signals, such as SGMII TX/RX and the 125MHz LVDS clock, connect to gigabit transceivers that are independent of the VADJ voltage used and do not need voltage translation.

The I/O power supply of the TI DP83867 Ethernet PHYs is connected to 3.3VDC.

SGMII

The Serial GMII interfaces form the connection between the Ethernet PHYs and the MACs that are implemented in the FPGA or SoC on the development board. The SGMII interface is serial gigabit interface composed of two differential pairs, one for transmit and one for receive. The SGMII interfaces connect to the first four gigabit transceivers of the FMC connector (DP0-3).

Port	Signal direction	FMC gigabit transceiver
P0	FPGA to link partner	DP0_C2M_P/N
	Link partner to FPGA	DP0_M2C_P/N
P1	FPGA to link partner	DP1_C2M_P/N
	Link partner to FPGA	DP1_M2C_P/N
P2	FPGA to link partner	DP2_C2M_P/N
	Link partner to FPGA	DP2_M2C_P/N
P3	FPGA to link partner	DP3_C2M_P/N
	Link partner to FPGA	DP3_M2C_P/N

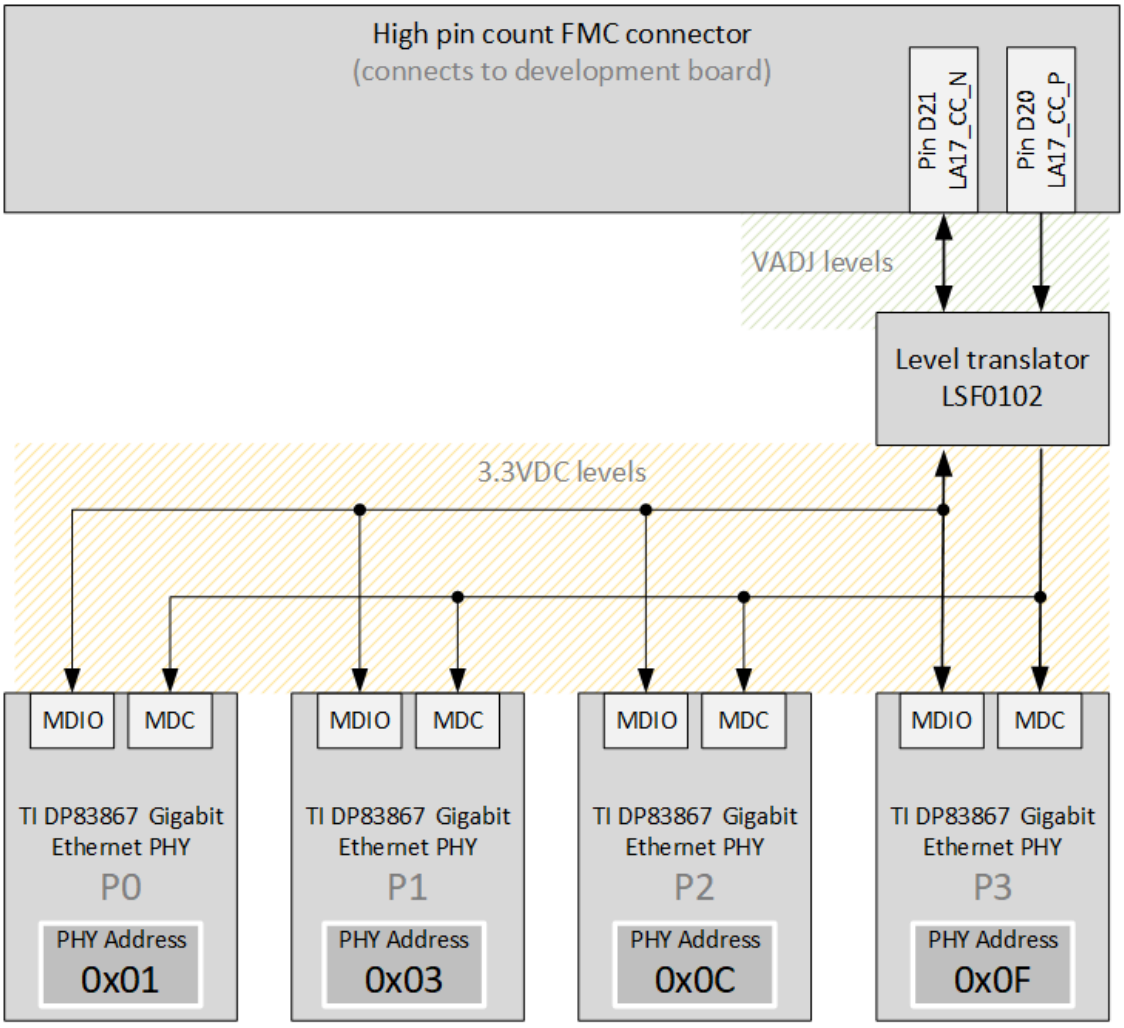
As the SGMII signals connect to gigabit transceivers, they are independent of the VADJ voltage being used and do not need voltage translation.

MDIO (PHY Configuration)

The MDIO interface is used to configure the registers of the Ethernet PHYs. More information regarding the registers can be found in the DP83867 datasheet.

The mezzanine card has a single shared MDIO bus to allow configuration of the PHYs. A level translator (LSF0102DQER) converts the VADJ voltage levels on the side of the FPGA to the 3.3VDC voltage levels on the side of the PHYs. The MDIO bus is composed of two signals:

- MDIO Clock signal (driven by the FPGA)
- MDIO Data signal (bidirectional)



MDIO bus

The diagram above illustrates the MDIO bus connections and the level translation. Note that the MDIO pull up resistors are left out of the diagram for simplicity.

The table below lists the MDIO bus signals and their connections to the FMC connector.

Bus signal	Description	Direction	FMC pin
MDC	MDIO clock	FPGA to PHY	LA17_CC_P
MDIO	MDIO data	Bidirectional	LA17_CC_N

Each Ethernet PHY has a fixed address that is used when targetting the PHY for MDIO transactions. The table below lists the ports and the corresponding PHY addresses:

Port label	PHY address (binary)	PHY address (hex)
P0 (Port 0)	00000001	0x01
P1 (Port 1)	00000011	0x03
P2 (Port 2)	00001100	0x0C
P3 (Port 3)	00001111	0x0F

The DP83867 datasheet specifies a maximum MDIO clock frequency of 25MHz.

PHY Resets

Each of the 4x Ethernet PHYs have an active-low reset input that can be driven (optionally) by the FPGA to hard reset the PHY. The reset signals have pull-up resistors to ensure that the PHYs are released from reset in the case that the FPGA leaves these pins floating or does not drive them. The reset signals pass through a level translator (SN74AVC4T245RSVR) to convert the VADJ signal levels from the FPGA to the 3.3V signal levels of the PHY.

The resets are connected to the following FMC pins:

Port label	Reset signal name	FMC pin
P0 (Port 0)	E0_RESET_N_T	LA12_P
P1 (Port 1)	E1_RESET_N_T	LA12_N
P2 (Port 2)	E2_RESET_N_T	LA11_P
P3 (Port 3)	E3_RESET_N_T	LA11_N

PHY GPIO Outputs

Each of the Ethernet PHYs have two multi-purpose outputs labelled GPIO_0 and GPIO_1. Despite the name “GPIO”, these pins can only be configured outputs to the PHY. Their operational mode can be configured by writing to GPIO Mux Control Register (GPIO_MUX_CTRL, address 0x0172) of the PHYs (see the DP83867 datasheet for more information). The GPIO outputs can signal such events as Wake-on-LAN, 1588 Start of Frame and receive errors. Level translators (SN74AVC4T245RSVR) are used to convert the 3.3V levels from the PHY to VADJ levels required by the FPGA.

By default, the GPIO outputs have the following functionality:

GPIO	Output	Description

GPIO_0	RX_ER	Receive error
GPIO_1	COL	Collision detect

The GPIO pins are connected to the following FMC pins for use by the FPGA:

Port	Net	Description	FMC pin
P0 (Port 0)	E0_GPIO0_T	PHY GPIO0 output	LA08_P
P0 (Port 0)	E0_GPIO1_T	PHY GPIO1 output	LA08_N
P1 (Port 1)	E1_GPIO0_T	PHY GPIO0 output	LA07_P
P1 (Port 1)	E1_GPIO1_T	PHY GPIO1 output	LA07_N
P2 (Port 2)	E2_GPIO0_T	PHY GPIO0 output	LA16_P
P2 (Port 2)	E2_GPIO1_T	PHY GPIO1 output	LA16_N
P3 (Port 3)	E3_GPIO0_T	PHY GPIO0 output	LA15_P
P3 (Port 3)	E3_GPIO1_T	PHY GPIO1 output	LA15_N

LVDS Clock

The Ethernet FMC Max has a 125MHz crystal oscillator (Skyworks, Si511) to provide the FPGA gigabit transceivers with a reference clock that meets all stability and jitter specifications for Gigabit Ethernet. The oscillator outputs an LVDS clock and connects to the pins listed in the table below:

Clock signal	Si511 pin	FMC pin
125MHz LVDS positive	CLK_P	GBTCLK0_M2C_P
125MHz LVDS negative	CLK_N	GBTCLK0_M2C_N

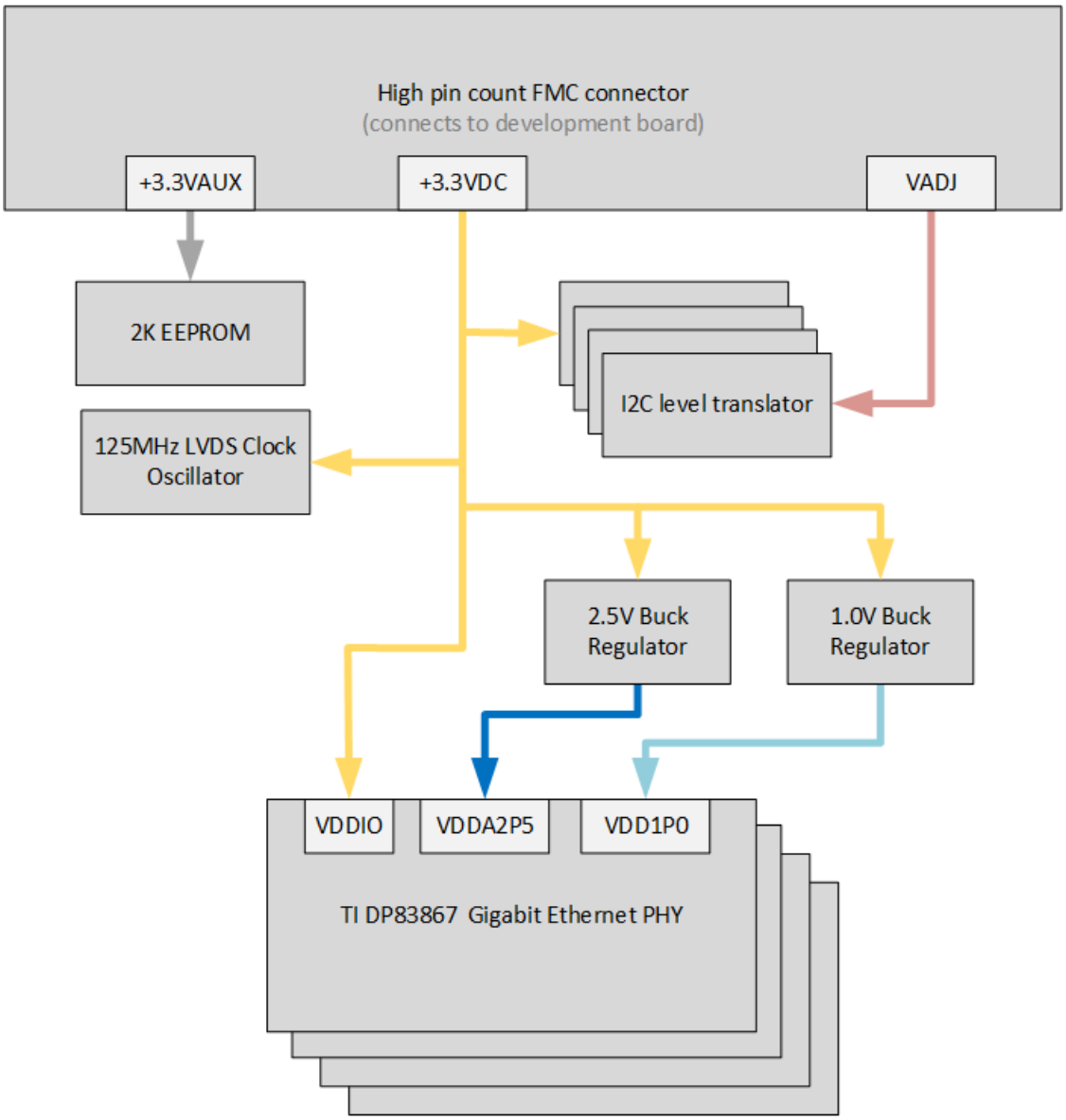
Power Supplies

All power required by the Ethernet FMC Max is supplied by the development board through the FMC connector:

- +12VDC
- +3.3VDC
- VADJ: 1.2VDC, 1.5VDC, 1.8VDC or 2.5VDC

- +3.3VAUX

Note that although the FMC standard provides for a 12VDC supply, the Ethernet FMC Max does not use that supply nor does it draw current from that supply.



Power supplies

3.3VDC Supply

The 3.3VDC supply is the main power supply for the Ethernet FMC Max, it is used to power the I/O power supply (VDDIO) of the 4x TI DP83867 PHYs, as well as the 125MHz clock oscillator. The 3.3VDC supply also feeds the buck converters that generate 1.0VDC and 2.5VDC that are also required by the Ethernet PHYs.

VADJ Supply

The VADJ supply is the FPGA I/O power supply and it determines the voltage levels of the FMC I/Os. The Ethernet FMC Max uses level translators on all applicable FPGA I/Os to allow a wide range of I/O voltages to be used. The Ethernet FMC Max can support a VADJ voltage of 1.2VDC, 1.5VDC, 1.8VDC or 2.5VDC.

Power LED and testpoints

A single green LED on the Ethernet FMC Max is used to indicate when the carrier board has signaled that the FMC power supplies are active. This LED is connected through a logic buffer to the POWER GOOD signal that is driven by the carrier board and is part of the Vita 57.1 FMC standard.

Note that this LED does not indicate whether the on-board buck regulators have also signaled “power good”. The POWER GOOD signals from the buck regulators are connected to I/Os LA13_P and LA13_N on the FMC connector so that the FPGA can read them.

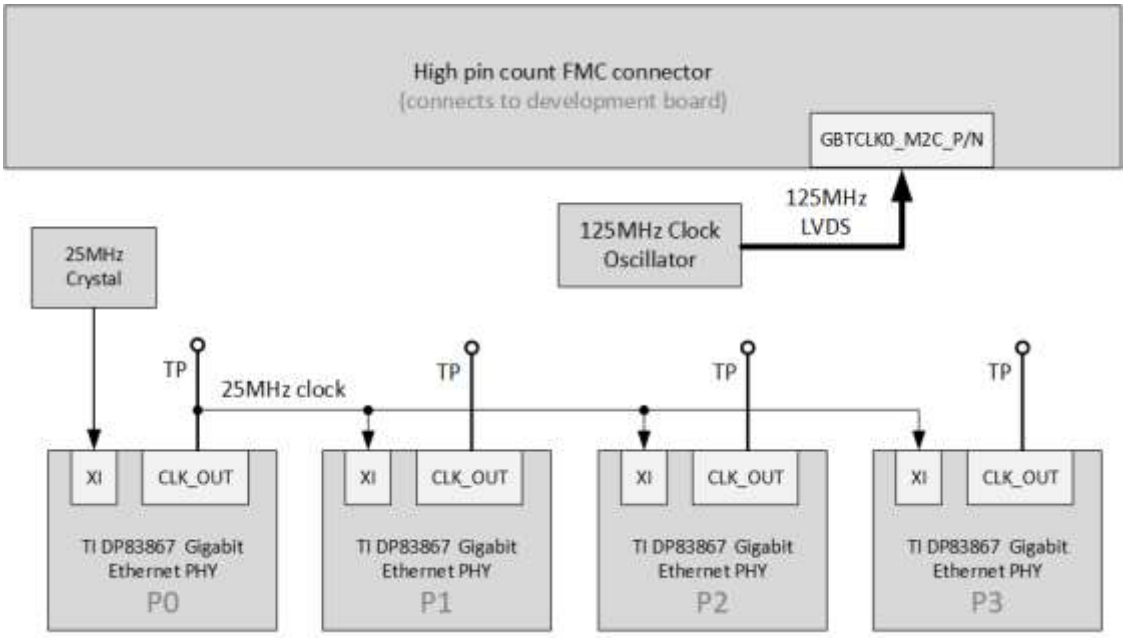
To aid hardware debug, there is a test point for the 3.3VDC, 1.0VDC and 2.5VDC power supplies on the back side of the Ethernet FMC Max. The testpoint labelled GND is connected to the system ground and should be used as the reference when probing the other testpoints. Note that the RJ45 connector chassis is connected to a chassis ground that is isolated from the system ground.

3.3VAUX Supply

The 3.3VAUX supply is used to power the IPMI EEPROM and is independent of the main 3.3VDC supply so that the carrier board can read from the EEPROM without having to power up the entire board.

Clocks

The figure below illustrates the clock connections on the Ethernet FMC Max.



Clocks

The PHY of the first port (P0) is connected to a 25MHz crystal for generation of it's own internal clocks. By default, the CLK_OUT pin of this PHY outputs a buffered 25MHz clock that is synchronous to the crystal input. This clock output is connected to the XI (clock input) pins of the remaining 3 PHYs.

The CLK_OUT outputs are not routed to the FMC connector and are not available to the FPGA. They are however connected to test points on the back side of the mezzanine card for debugging purposes. The CLK_OUT testpoints are unlabelled and are located in the region of the decoupling capacitors.

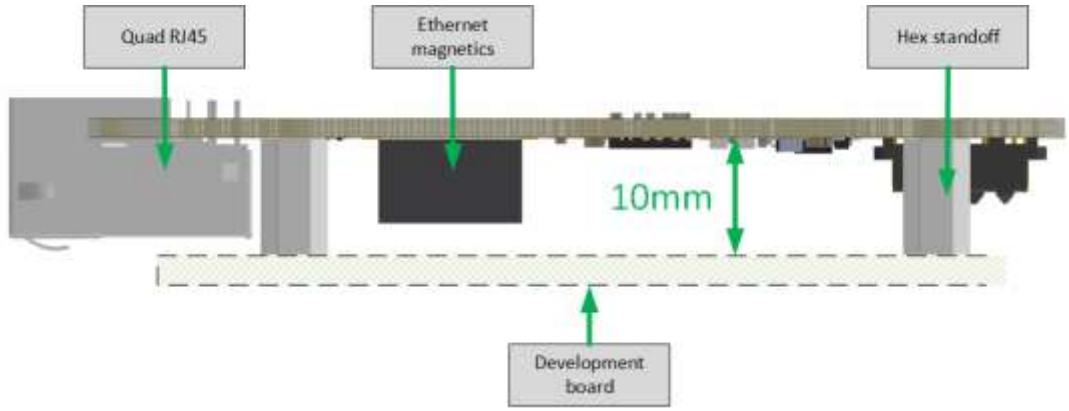
Note that this clock architecture depends on the PHY of the first port (P0) outputting a 25MHz clock through the CLK_OUT pin. This is the default behavior of the DP83867 PHY. Any changes to the operating mode of this pin through I/O Configuration register (address 0x0170) may result in a failure of the PHYs P1,P2 and P3.

The Ethernet FMC Max also has a 125MHz clock oscillator with LVDS output to provide the FPGA gigabit transceivers with a precision reference clock.

Mechanical Information

Height Profile

The figure below illustrates the height profile of the Ethernet FMC Max. All of the components on the Ethernet FMC Max fit within the 10mm gap between the FMC card and the development board.

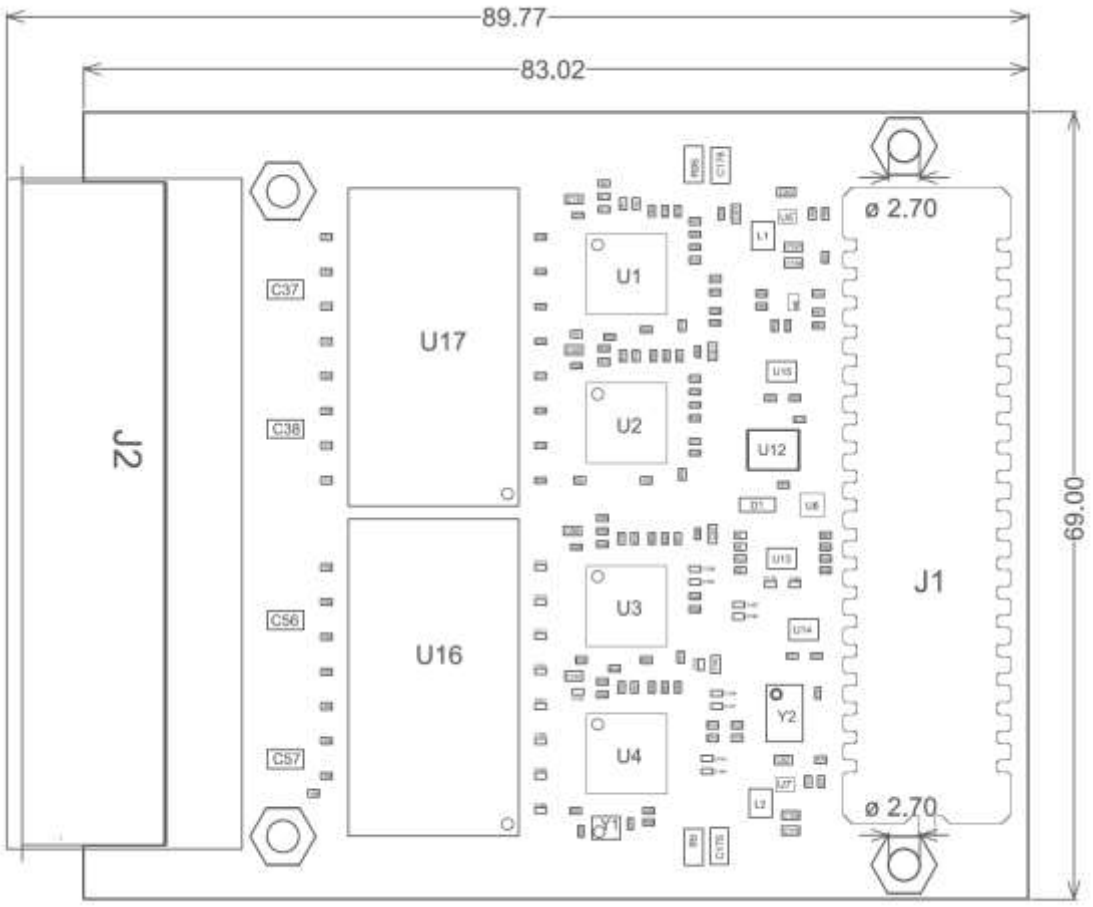


Ethernet FMC Max height profile (view from side)

Dimensions

The mechanical dimensions of the Ethernet FMC Max are illustrated in the figure below. All dimensions are in millimeters (mm).

The assembly drawings are also available as PDF files that you can download at the provided links.



Ethernet FMC Max mechanical drawing

- Ethernet FMC Max Rev-A Assembly Drawing PDF

3D Model

The 3D model of the board is available as a STEP file at the links below:

- Ethernet FMC Max Rev-A 3D STEP model

Mezzanine fastening hardware

For mechanical fastening of the mezzanine card to the carrier board, the Ethernet FMC Max comes with 2x hex standoffs. We **highly recommend** using the machine screws on each of these standoffs to fix the mezzanine card to the carrier board. If the fastening screws are misplaced, they can be replaced by the ones listed below, or equivalents.

The hex standoff and machine screw part numbers are listed below:

- Hex standoff, Thread M2.5 x 0.45, Brass, Board-to-board length 10mm
  Part number: V6516C
  Manufacturer: Assmann
- Machine screw, Thread M2.5 x 0.45, Length (below head) 4mm, Stainless steel, Phillips head
  Part number: 90116A105
  Supplier: McMaster-Carr

Getting Started

Minimum setup

To develop with the Ethernet FMC Max, we recommend you start by getting your hands on the minimum hardware and software requirements:

3. An FPGA or MPSoC development board - make sure that it is on our list of compatible boards.
4. An Ethernet FMC Max to match the dev board.
5. A license for the Xilinx TEMAC IP (unless you want to use something else, see below section on getting a license).
6. Build and run one of our example designs.

Support for other devices: Note that all of our example designs were developed using Xilinx software tools and the Xilinx AXI Ethernet Subsystem IP. Although it is possible to use the Ethernet FMC Max with FPGA devices from other chip makers such as Intel/Altera, our example designs will not work on these devices and our ability to provide technical support for these other devices is limited at the current time.

Getting a license for the Xilinx Tri-mode Ethernet MAC

When do I need a license?

- You want to use the example designs provided on this website that are based on the Xilinx soft TEMAC. (which is all of them at this point in time)
- You want to create your own designs that are based on the Xilinx soft TEMAC. Using the Xilinx soft TEMAC can save you a considerable amount of time because you benefit from all the Xilinx support including example designs, documentation and drivers.

When do I NOT need a license?

- You want to create your own designs that are **not** based on the Xilinx soft TEMAC.
  Your options: Design your own TEMAC, purchase a 3rd party TEMAC, or use the open source TEMAC on opencores.org.
- You are using the Virtex®-4 FX or Virtex-5 LXT/SXT, which contain hard TEMACs.
  AND your device contains a sufficient number of them to support your application. If you need 4 ports, you must have 4 hard TEMACs in your device.

License types

Evaluation license

An evaluation license allows you to do everything you can do with the fully licensed IP core, including configuration, simulation and bitstream generation. You can also test the IP core on hardware, however it will cease to function after a certain period of time (typically 8 hours).

To obtain an evaluation license, visit Xilinx TEMAC Evaluation and click on the link Generate Soft TEMAC License Key. You will have to log into the Xilinx website, select the TEMAC evaluation license and click “Generate license”. Xilinx will then send you the license by email with instructions for how to install it.

Full license

The full license can be purchased as a “site” or “project” license. The project license limits use of the IP core to one project, generally meaning one bitstream, or one printed circuit board. The site license can be used on an unlimited number of projects however is limited to a single company site.

- **Project license part number:** *EF-DI-TEMAC-PROJ*
- **Site license part number:** *EF-DI-TEMAC-SITE*

Both licenses can be purchased from Xilinx here. Alternatively you can search the part numbers on Avnet and Digikey websites.

Compatible Boards

This section of the documentation aims to list all of the development boards for which compatibility with the Ethernet FMC Max has been checked, and to list constraints and any notes concerning special requirements or limitations with the board.

List of boards

The following development boards have been verified compatible with the Ethernet FMC Max. For more detailed information regarding compatibility with a particular development board, including the availability of an example design, click on the name of the board in the table below.

Note that we are still working on the reference designs for these boards and we expect them to be available by September 2024.

Series-7 boards

Carrier	FMC	Compatible	Ref design	Supported Ports
AMD Xilinx KC705 Kintex-7 Development board	HPC	✔	Coming soon	4
AMD Xilinx KC705 Kintex-7 Development board	LPC	✔	No	1 [1]
AMD Xilinx VC707 Virtex-7 Development board	HPC1	✔	Coming soon	4
AMD Xilinx VC707 Virtex-7 Development board	HPC2	✔	Coming soon	4
AMD Xilinx VC709 Virtex-7 Development board	HPC	✔	Coming soon	4
AMD Xilinx ZC706 Zynq-7000 Development board	HPC	✔	Coming soon	4

[1] LPC connectors can only support 1-lane PCIe

AMD Xilinx ZC706 Zynq-7000 Development board	LPC	✔	No	1 [2]
Avnet PicoZed FMC Carrier Card V2 Zynq-7000 Development Board	LPC	✔	No	1 [3]

UltraScale boards

Carrier	FMC	Compatible	Ref design	Supported Ports
AMD Xilinx KCU105 Kintex UltraScale Development board	HPC	✔	Coming soon	4
AMD Xilinx KCU105 Kintex UltraScale Development board	LPC	✔	No	1 [4]
AMD Xilinx VCU108 Virtex UltraScale Development board	HPC0	✔	Coming soon	4
AMD Xilinx VCU108 Virtex UltraScale Development board	HPC1	✔	Coming soon	4

Zynq Ultrascale+ boards

Carrier	FMC	Compatible	Ref design	Supported Ports
AMD Xilinx ZCU104 Zynq UltraScale+ Development board	LPC	✔	No	1 [5]
AMD Xilinx ZCU102 Zynq UltraScale+ Development board	HPC0	✔	Coming soon	4
AMD Xilinx ZCU102 Zynq UltraScale+ Development board	HPC1	✔	Coming soon	4

[2] LPC connectors can only support 1-lane PCIe

[3] LPC connectors can only support 1-lane PCIe

[4] LPC connectors can only support 1-lane PCIe

[5] LPC connectors can only support 1-lane PCIe

AMD Xilinx ZCU106 Zynq UltraScale+ Development board	HPC0	✔	Coming soon	4
AMD Xilinx ZCU106 Zynq UltraScale+ Development board	HPC1	✔	No	1
AMD Xilinx ZCU111 Zynq UltraScale+ Development board	FMC+	✔	Coming soon	4
AMD Xilinx ZCU208 Zynq UltraScale+ Development board	FMC+	✔	Coming soon	4
Avnet UltraZed EV Carrier Zynq UltraScale+ Development board	HPC	✔	Coming soon	4
Trenz UltraITX+ Baseboard Zynq UltraScale+ Development board	HPC	✔	Coming soon	4

Ultrascale+ boards

Carrier	FMC	Compatible	Ref design	Supported Ports
AMD Xilinx VCU118 Virtex UltraScale+ Development board	HPC	✘ Use FMC+ instead	No	Not supported
AMD Xilinx VCU118 Virtex UltraScale+ Development board	FMC+	✔	Coming soon	4

Versal boards

Carrier	FMC	Compatible	Ref design	Supported Ports
AMD Xilinx VCK190 Versal AI Core Development board	FMC+1	✔	Coming soon	4
AMD Xilinx VCK190 Versal AI Core Development board	FMC+2	✔	Coming soon	4
AMD Xilinx VMK180 Versal Prime Series Development board	FMC+1	✔	Coming soon	4

AMD Xilinx VMK180 Versal Prime Series Development board	FMC+2	✔	Coming soon	4
AMD Xilinx VPK120 Versal Premium Series Development board	FMC+	✔	Coming soon	4

Compatibility requirements

If you need to determine the compatibility of a development board that is not listed here, or you are designing a carrier board to mate with the Ethernet FMC Max, please check your board against the list of requirements below.

VADJ

The development board must have the ability to supply a VADJ voltage between 1.2VDC and 2.5VDC. The Ethernet FMC Max has an EEPROM containing IPMI data to be used by a power management device. If the development board has such a power management device, an appropriate VADJ voltage will be applied automatically on power-up. Note that some development boards require the VADJ voltage to be configured by a DIP switch or jumper placement.

Gigabit transceivers

The FPGA or MPSoC device must have gigabit transceivers and they must be routed to the FMC connector. The PHYs of ports 0-3 are routed to transceivers DP0-DP3 respectively and these transceivers must be connected to the FPGA for the Ethernet ports to work.

Port label	Signal direction	FMC Pin	FMC pin name
P0	Link partner to FPGA	C6/C7	DP0_M2C_P/N
	FPGA to Link partner	C2/C3	DP0_C2M_P/N
P1	Link partner to FPGA	A2/A3	DP1_M2C_P/N
	FPGA to Link partner	A22/A23	DP1_C2M_P/N
P2	Link partner to FPGA	A6/A7	DP2_M2C_P/N
	FPGA to Link partner	A26/A27	DP2_C2M_P/N
P3	Link partner to FPGA	A10/A11	DP3_M2C_P/N

FPGA to Link partner A30/A31 DP3_C2M_P/N

Note that low pin count (LPC) FMC connectors only have one possible GT connection (DP0). For this reason, carrier boards with LPC FMC connectors can only support a single Ethernet port (P0).

The GT clock reference (FMC pins GBTCLK0_M2C_P/N) should be connected to one of the GT reference clock inputs of the quad to which DP0-3 connect, or an adjacent quad.

Featured I/O

The following FMC pins should ideally be connected to the FPGA as they provide extra functionality to the mezzanine card. These pins are not critical to the operation of the mezzanine card; it can operate without them if they are not connected on the carrier board.

FMC Pin	FMC name	Net	Description
G15	LA12_P	E0_RESET_N_T	Port 0 PHY reset signal (active low)
G16	LA12_N	E1_RESET_N_T	Port 1 PHY reset signal (active low)
H16	LA11_P	E2_RESET_N_T	Port 2 PHY reset signal (active low)
H17	LA11_N	E3_RESET_N_T	Port 3 PHY reset signal (active low)
G12	LA08_P	E0_GPIO0_T	Port 0 PHY GPIO0 output
G13	LA08_N	E0_GPIO1_T	Port 0 PHY GPIO1 output
H13	LA07_P	E1_GPIO0_T	Port 1 PHY GPIO0 output
H14	LA07_N	E1_GPIO1_T	Port 1 PHY GPIO1 output
G18	LA16_P	E2_GPIO0_T	Port 2 PHY GPIO0 output
G19	LA16_N	E2_GPIO1_T	Port 2 PHY GPIO1 output
H19	LA15_P	E3_GPIO0_T	Port 3 PHY GPIO0 output
H20	LA15_N	E3_GPIO1_T	Port 3 PHY GPIO1 output
D20	LA17_CC_P	MDC	MDIO clock (shared bus)
D21	LA17_CC_P	MDIO	MDIO data (shared bus)

D17	LA13_P	PG_1V0	Power good output of 1.0V buck converter
D18	LA13_N	PG_2V5	Power good output of 2.5V buck converter

Programming Guide

This section provides the details of the programming requirements to operate the Ethernet FMC Max hardware and customise functionality.

PHY registers

The functionality of the TI DP83867 Gigabit Ethernet PHYs can be customized by writing to the registers of the device via the MDIO bus. These registers are detailed in the DP83867 datasheet.

To target a specific PHY for an MDIO transaction, use the MDIO addresses listed in the table below:

Port label	PHY address (binary)	PHY address (hex)
P0 (Port 0)	00000001	0x01
P1 (Port 1)	00000011	0x03
P2 (Port 2)	00001100	0x0C
P3 (Port 3)	00001111	0x0F

The tables below list some of the registers and settings that are useful for basic operation of the Ethernet FMC Max. For a comprehensive list of the registers, please refer to the DP83867 datasheet.

Register modes:

- R/W: Read and write
- RO: Read only
- SC: Self clearing
- LH: Latches high until read or reset occurs

Basic Mode Control Register (BMCR), Address 0x0000

Bits	Description	Mode	Default Value
15	Software reset	R/W, SC	0x0
12	Enable Auto-negotiation	R/W	0x1 (strap)

9	Restart Auto-negotiation	R/W, SC	0x0

Basic Mode Status Register (BMSR), Address 0x0001

Bits	Description	Mode	Default Value
5	Auto-negotiation Complete	RO	0x0

Auto-Negotiation Advertisement Register (ANAR), Address 0x0004

Bits	Description	Mode	Default Value
11	Asymmetric pause	R/W	0x0
10	MAC pause	R/W	0x0
8	Advertise 100BASE-TX full duplex support	R/W	0x1
7	Advertise 100BASE-TX support	R/W	0x1
6	Advertise 10BASE-Te full duplex support	R/W	0x1
5	Advertise 10BASE-Te support	R/W	0x1

Configuration Register 1 (CFG1), Address 0x0009

Bits	Description	Mode	Default Value
9	Advertise 1000BASE-T full duplex	R/W	0x1
8	Advertise 1000BASE-T half duplex	R/W	0x1

PHY Control Register (PHYCR), Address 0x0010

Bits	Description	Mode	Default Value
11	SGMII Enable	R/W	0x1 (Strap)

The SGMII enable setting is set to 1 by strap resistors on the Ethernet FMC Max; it does not need to be set by software.

PHY Status Register (PHYSTS), Address 0x0011

Bits	Description	Mode	Default Value

15:14	Established link speed Valid only when speed and duplex resolved asserted (bit 11) 10b = 1Gbps 01b = 100Mbps 00b = 10Mbps	RO	0x2
11	Speed and duplex resolved	RO	0x0

Interrupt Status Register (ISR), Address 0x0013

Bits	Description	Mode	Default Value
15	Auto-negotiation Error	RO, LH	0x0

Configuration Register 2 (CFG2), Address 0x0014

Bits	Description	Mode	Default Value
7	SGMII Auto-Negotiation Enable	RW	0x1

Configuration Register 4 (CFG4), Address 0x0031

Bits	Description	Mode	Default Value
6:5	SGMII Auto-negotiation timer duration 00 = 11 ms 10 = 800 us 01 = 2 us 00 = 16ms	RW	01
0	Port Mirror Enable	RW	Strap

Note that the Port Mirror Enable bit default setting is determined by the strap resistors. On the Ethernet FMC Max Rev-A, (serial numbers 800000-800019) the strap resistors set this to 0 (Mirror mode disabled). When using Rev-A boards, this bit must be set to 1 by software for proper operation of the Ethernet ports. Our reference designs contain the software to ensure that Mirror Mode is enabled.

SGMII Control Register 1 (SGMIICTL1), Address 0x00D3

Bits	Description	Mode	Default Value
14	SGMII Configuration 1 = 6-wire mode 0 = 4-wire mode	RW	0x0

The SGMII Configuration should be set to 0x0 (4-wire mode) for the Ethernet FMC Max. This is the default setting and does not require setting by software.

Extended Address Space Access

All PHY registers above address 0x001F are in the extended address space and must be accessed using registers REGCR (0x000D) and ADDAR (0x000E). The procedure for accessing registers in the extended address space is described in the DP83867 datasheet. The code snippets below can be used as examples of reading and writing to the extended register space:

Extended Register Read Function

```
/*
 * Read from PHY extended register (address above 0x001F)
 */
void XAxiEthernet_PhyReadExtended(XAxiEthernet *InstancePtr, u32 PhyAddress,
                                  u32 RegisterNum, u16 *PhyDataPtr)
{
    XAxiEthernet_PhyWrite(InstancePtr, PhyAddress,TI_PHY_REGCR, 0x001F);
    XAxiEthernet_PhyWrite(InstancePtr, PhyAddress,TI_PHY_ADDDR, RegisterNum);
    XAxiEthernet_PhyWrite(InstancePtr, PhyAddress,TI_PHY_REGCR, 0x401F);
    XAxiEthernet_PhyRead(InstancePtr, PhyAddress,TI_PHY_ADDDR, PhyDataPtr);
}
```

Extended Register Write Function

```
/*
 * Write to PHY extended register (address above 0x001F)
 */
void XAxiEthernet_PhyWriteExtended(XAxiEthernet *InstancePtr, u32 PhyAddress,
                                   u32 RegisterNum, u16 PhyDataPtr)
{
    XAxiEthernet_PhyWrite(InstancePtr, PhyAddress,TI_PHY_REGCR, 0x001F);
    XAxiEthernet_PhyWrite(InstancePtr, PhyAddress,TI_PHY_ADDDR, RegisterNum);
    XAxiEthernet_PhyWrite(InstancePtr, PhyAddress,TI_PHY_REGCR, 0x401F);
    XAxiEthernet_PhyWrite(InstancePtr, PhyAddress,TI_PHY_ADDDR, PhyDataPtr);
}
```

EEPROM

The 2K EEPROM is intended to store information that identifies the mezzanine card and also specifies the power supplies required by the card. This information is typically read by the system power management on the carrier board when it is powered up. In typical user applications, it should not be necessary to read the data on the EEPROM, and we highly recommend against writing to the EEPROM. Nevertheless, if you wish to access the EEPROM, it can be read and written to at the I2C address 0x50.

A6	A5	A4	A3	A2	A1	A0	Hexadecimal
1	0	1	0	0	0	0	0x50

The EEPROM sits on the FMC card's dedicated I2C bus. The FMC pins of the EEPROM's I2C bus are shown below, and it is up to the user to determine their corresponding connections to the FPGA/MPSoC on the carrier board being used.

I2C bus signal	FMC pin name	FMC pin number
SCL (clock)	SCL	C30
SDA (data)	SDA	C31

Be aware that on some carrier boards, the FMC I2C bus passes through an I2C MUX. On some boards it connects to FPGA pins whereas on others it connects to PS pins. If you wish to communicate with the EEPROM, it is necessary to check the schematic drawing of your carrier board to determine the structure of the I2C bus and to which pins it connects.

FMC EEPROM Tool

The Opsero FMC EEPROM Tool can be used to verify, reprogram or update the EEPROM contents of Opsero FMC products using an FPGA or MPSoC board such as the ZCU102 or VCU118 board.

Only use this tool with Opsero FMC products. The use of this tool with FMCs from other manufacturers is strictly prohibited and may result in damage to the FMC or to the carrier board.

Supported boards

The tool currently supports the following FPGA/MPSoC boards. You must have at least one of these boards in order to use the tool.

- KC705
- KCU105
- VCU118
- VCK190
- VMK180
- ZedBoard
- ZCU102 Rev1.0 and Rev1.1
- ZCU104
- ZCU106

Download

The tool can be downloaded at the link below:

Opsero FMC EEPROM Tool v1.5

The zip file contains a boot file (bitstream or BOOT.bin) for each of the supported boards.

Usage instructions

To run the tool, follow these steps:

1. Plug the FMC card you wish to reprogram into one of the FMC connectors of your FPGA/MPSoC board. The tool is designed to probe all of the FMC connectors on the FPGA/MPSoC board.
2. If you are using the ZedBoard, be sure to set the VADJ jumper setting to 1.8V. If you are using the KC705, be sure that your FMC card can support a VADJ of 2.5V, which is the default setting of that board.
3. Connect the UART of your FPGA/MPSoC board to a PC.
4. For Zynq and Zynq MP boards, a BOOT.bin file is provided. Copy this file to your board's SD card and configure it to boot from SD card. Then plug the SD card back into the board and power it up.
5. For FPGA boards, a bitstream is provided with an embedded ELF file. Power up your FPGA/MPSoC board and then download the bitstream to the FPGA board using the Vivado Hardware Manager tool.
6. Open a terminal program such as Putty and connect to the serial port of your FPGA/MPSoC board. If you see nothing in the terminal window, press ENTER to redisplay the menu.
7. Use the menu options to do the following:
   - **Program the EEPROM (p)**
     You will be asked to select the FMC product from a list, and also to enter the product's serial number. Note that entering incorrect information here can lead to your FMC card being damaged by a VADJ voltage that is greater than it's true rating. If you are not sure about the product to select here, please contact Opsero first.

Troubleshooting

This section describes some of the common issues that can arise when using the mezzanine card.

Auto-negotiation not working

Many issues can lead to a failure to auto-negotiate a link. Here are some of the most common issues that can occur:

Mirror Mode not enabled (Rev-A only)

Problem:

The Ethernet FMC Max requires Mirror Mode to be enabled in the TI PHY (DP83867, Port Mirror Enable bit 0 in CFG4 register address 0x0031). In the Rev-A boards (serial numbers 800000-800019), this option is not enabled by the strap resistors and must be enabled by software.

Solution:

If you have a Rev-B or more recent revision board, Mirror Mode is enabled by strap resistors, so you should not have to enable it by software.

If you have a Rev-A board, our reference designs already include the software required to enable Mirror Mode. If you have built your own custom design, you will need to add software to enable Mirror Mode in the PHY. This can be done by writing a 1 to bit 0 of PHY register CFG4 at address 0x0031 (note that this register is in the extended address space). If you are using Linux, you can refer to our reference design for a patch to the DP83867 driver that will allow you to enable Mirror Mode via the device tree.

Board Revision History

Rev A

- First board release

References

Board Files

Rev-A

- Ethernet FMC Max Rev-A Schematics PDF
- Ethernet FMC Max Rev-A Assembly Drawing PDF
- Ethernet FMC Max Rev-A 3D STEP model

Part Datasheets

Use the links below to access the datasheets of the significant parts on the mezzanine card.

- Samtec, Mezzanine-side High pin count FMC Connector, ASP-134488-01
- Link-PP, Quad RJ45, LPJE4718AGNL
- TI, 10/100/1000 Ethernet PHY, DP83867ISRGZ
- TI, 1A Step Down Converter, TLV62568APDRLR
- Skyworks, Crystal Oscillator 125MHz, 511BBA125M000BAG
- ON Semi, TinyLogic ULP-A Dual Buffer, NC7WV16P6X
- Link-PP, Quad Ethernet Magnetics, LP84862ANL
- TI, Voltage Translator, SN74AVC4T245RSVR

Revision History

Date	Version	Description
2024-09-27	1.0	Initial PDF release.

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