

REV.	DESCRIPTION	DATE	APPROVED
B-1	Changed package of I2C translators	2026-02-03	J Johnson



Standoff, Hex, 10mm, M2.5



Standoff, Hex, 10mm, M2.5

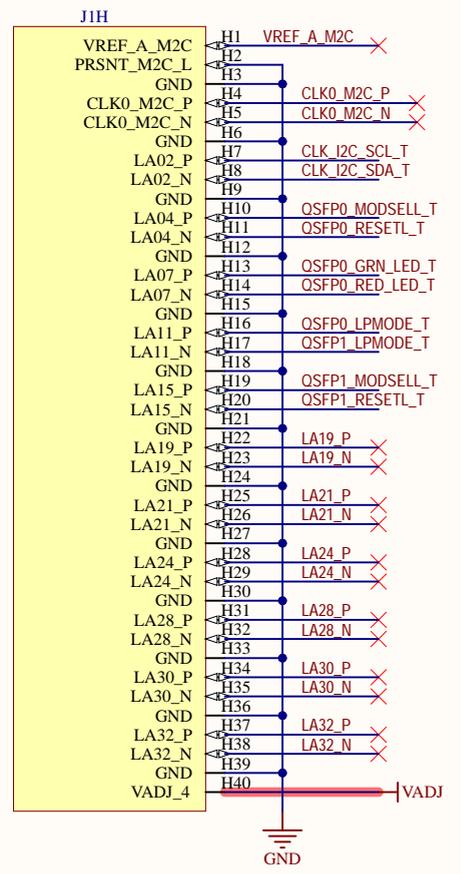
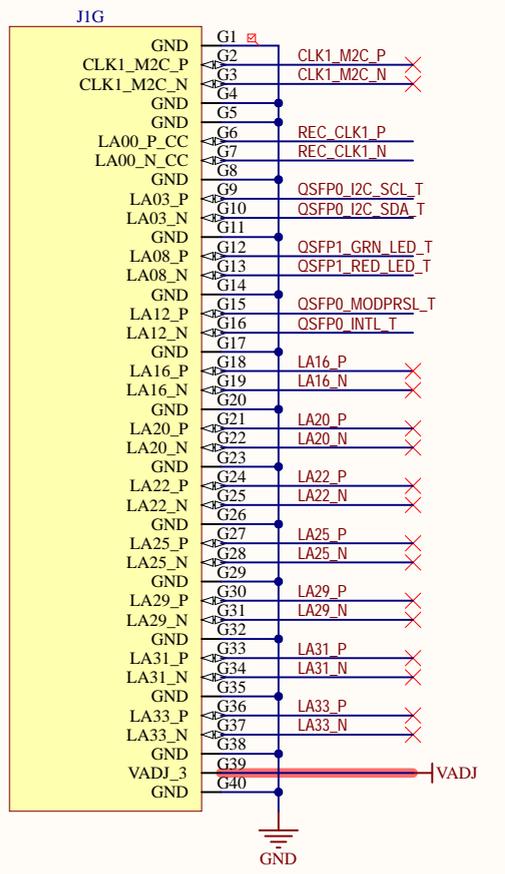
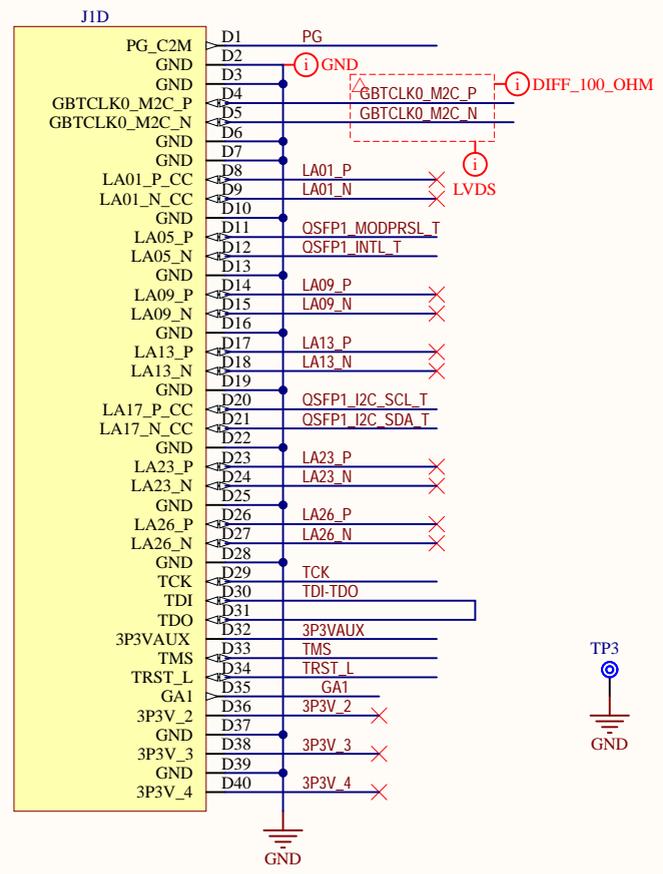
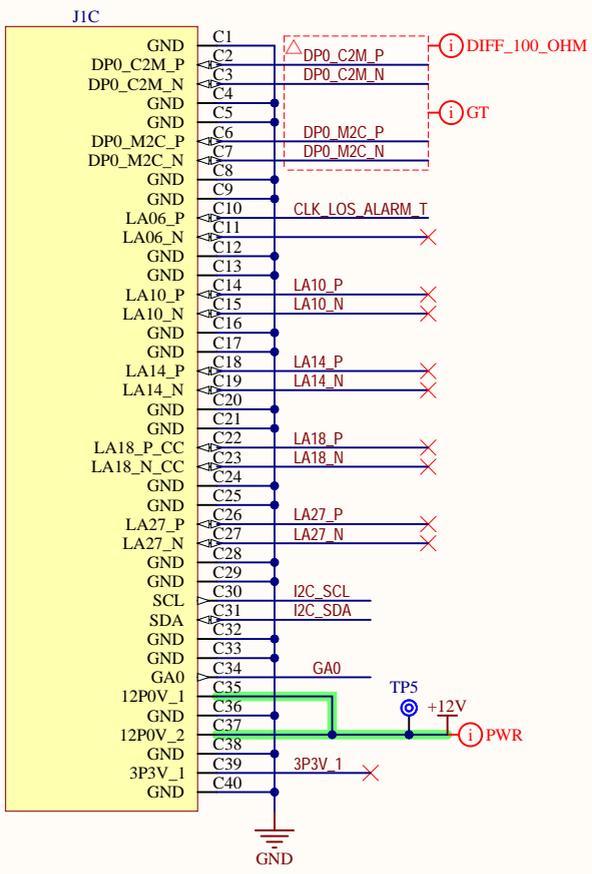


Machine Screw, M2.5 thread, 4mm length

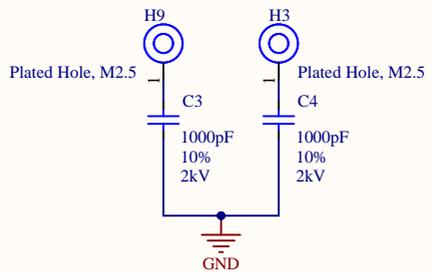


Machine Screw, M2.5 thread, 4mm length

# FMC PINS COMMON WITH LPC



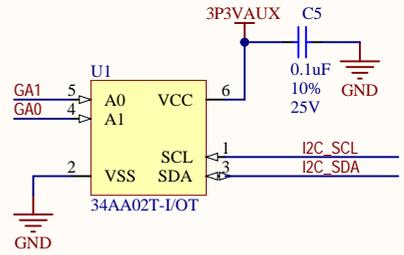
## MOUNTING HOLES



## FIDUCIALS



## EEPROM

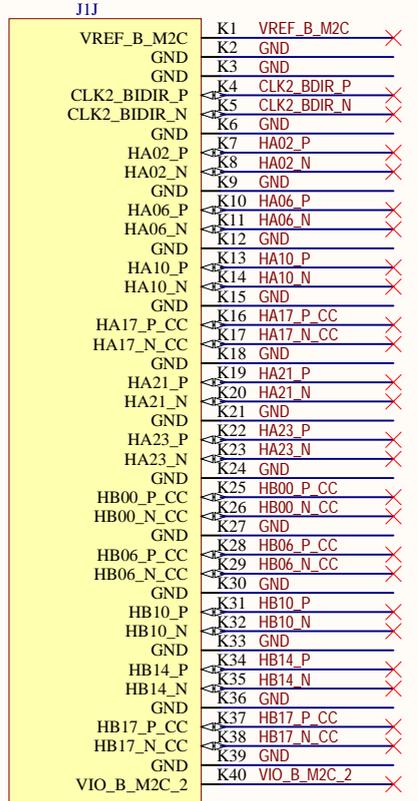
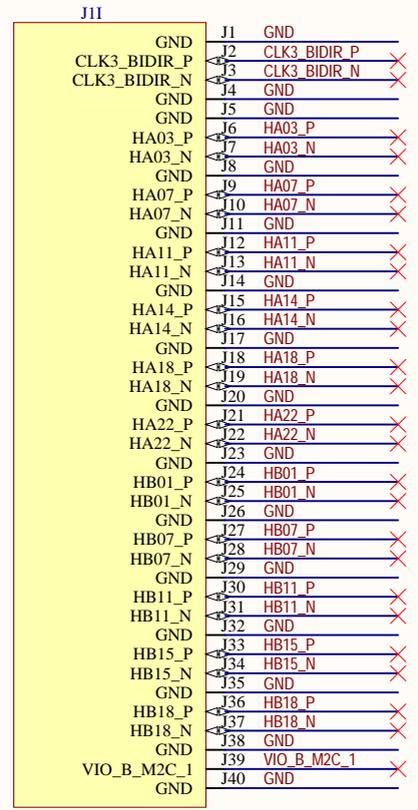
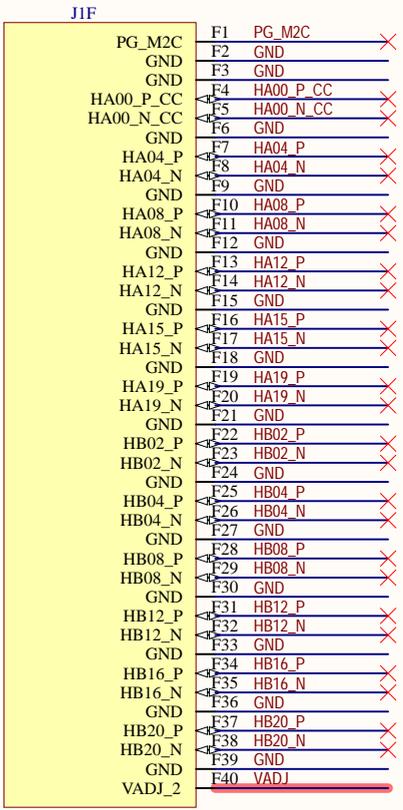
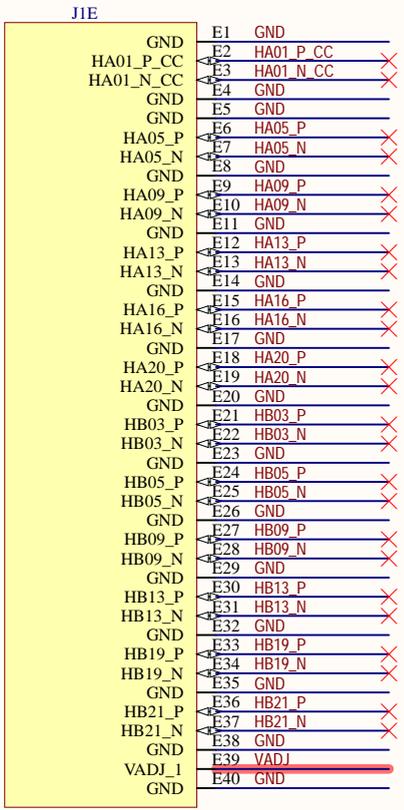
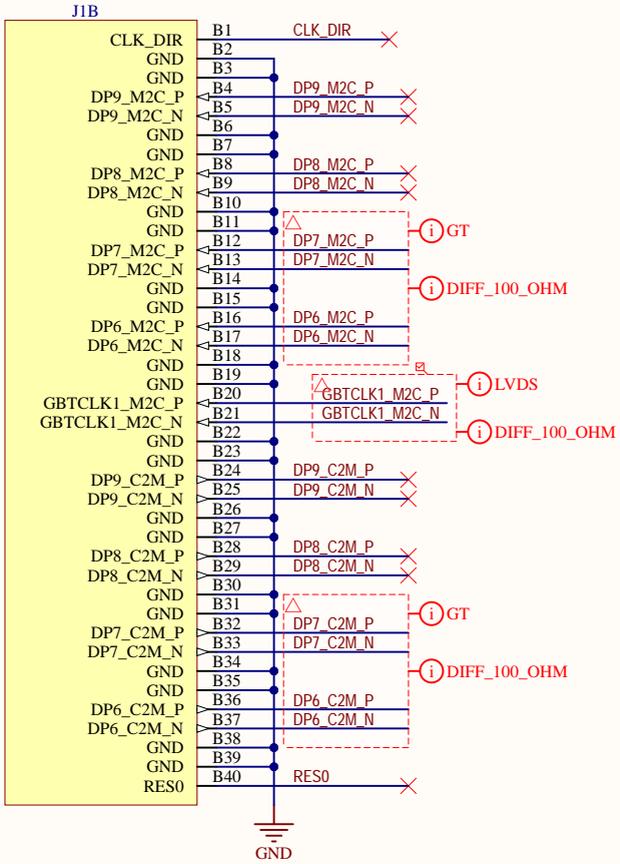
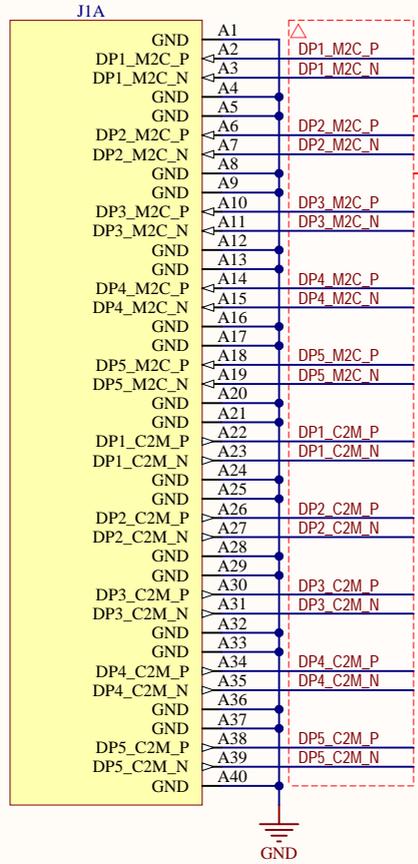


In accordance with the VITA 57.1 standard:  
GA0 goes to A1, GA1 goes to A0

TITLE: 2x QSFP28 FMC			
SHEET: LPC FMC			
CONFIG: Standard			
PROJECT: Ethernet FMC	DRAWN: J Johnson	DATE: 2025-02-24	
SIZE: B	SCH PIN: OP120-01-SCH.	REV: B-1	SHEET OF: 1 5

REV.	DESCRIPTION	DATE	APPROVED
B-1	Changed package of I2C translators	2026-02-03	J Johnson

### HPC FMC PINS

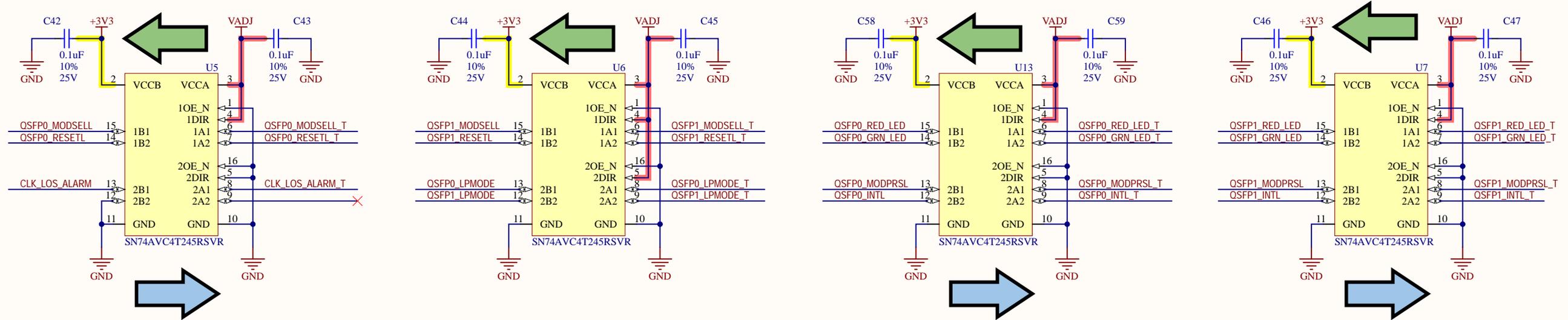


TITLE		2x QSFP28 FMC	
SHEET		HPC FMC	
CONFIG.		Standard	
PROJECT	Ethernet FMC	DRAWN	J Johnson
		DATE	2025-02-24
SIZE	SCH PIN.	REV.	SHEET
B	OP120-01-SCH.	B-1	2 OF 5

REV.	DESCRIPTION	DATE	APPROVED
B-1	Changed package of I2C translators	2026-02-03	J Johnson

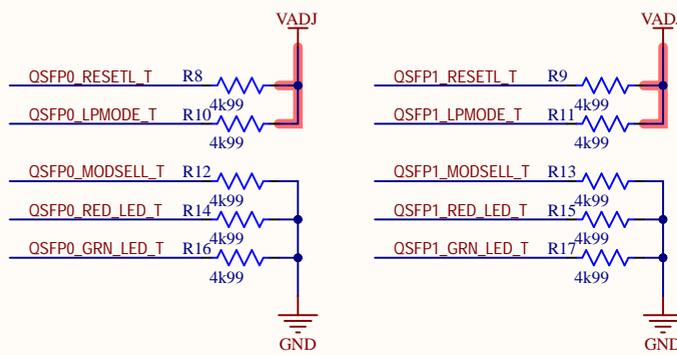
DIR	SIGNAL
INPUT	FLOW
LOW	B -> A
HIGH	A -> B

## VOLTAGE TRANSLATION

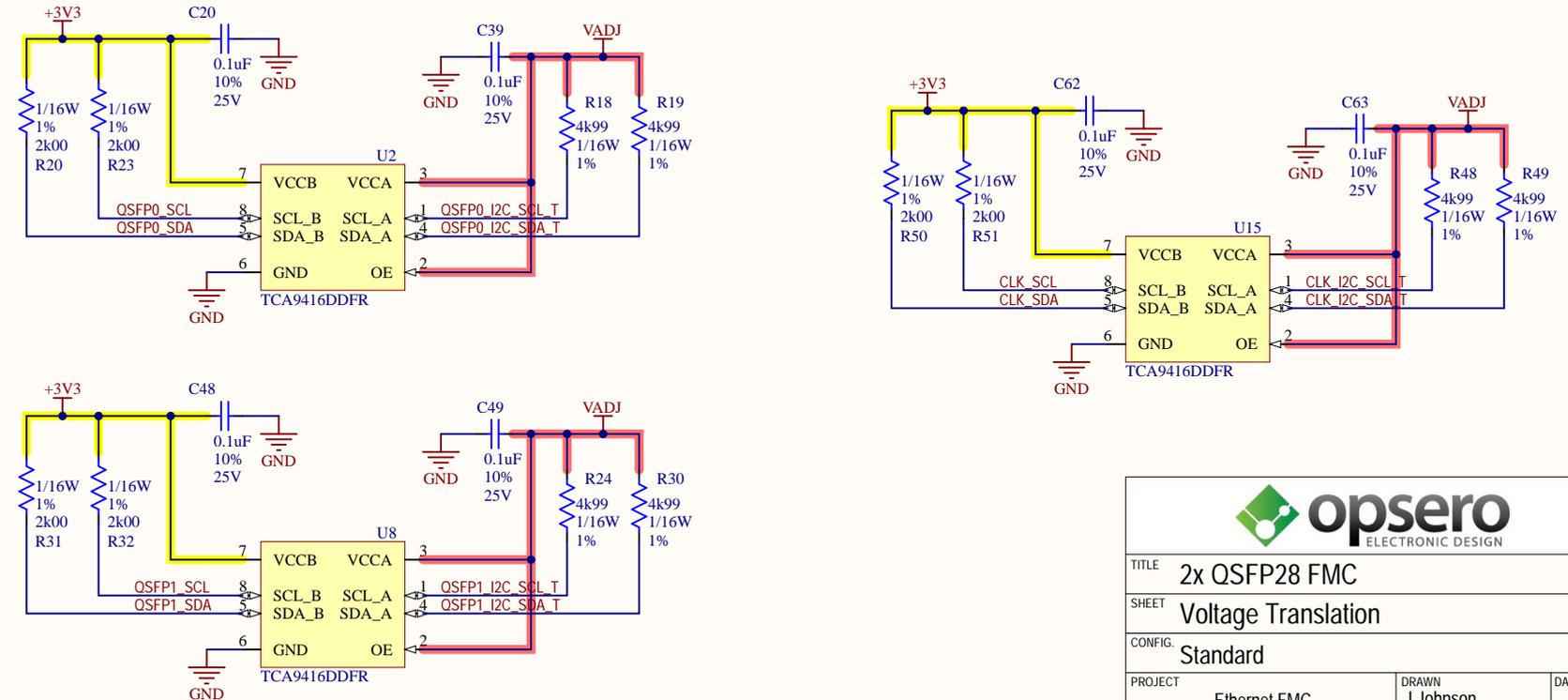


## I2C VOLTAGE TRANSLATION

### DEFAULTS



OSFP inputs are pulled to default levels in case the FMC pins have not been connected in the FPGA design.



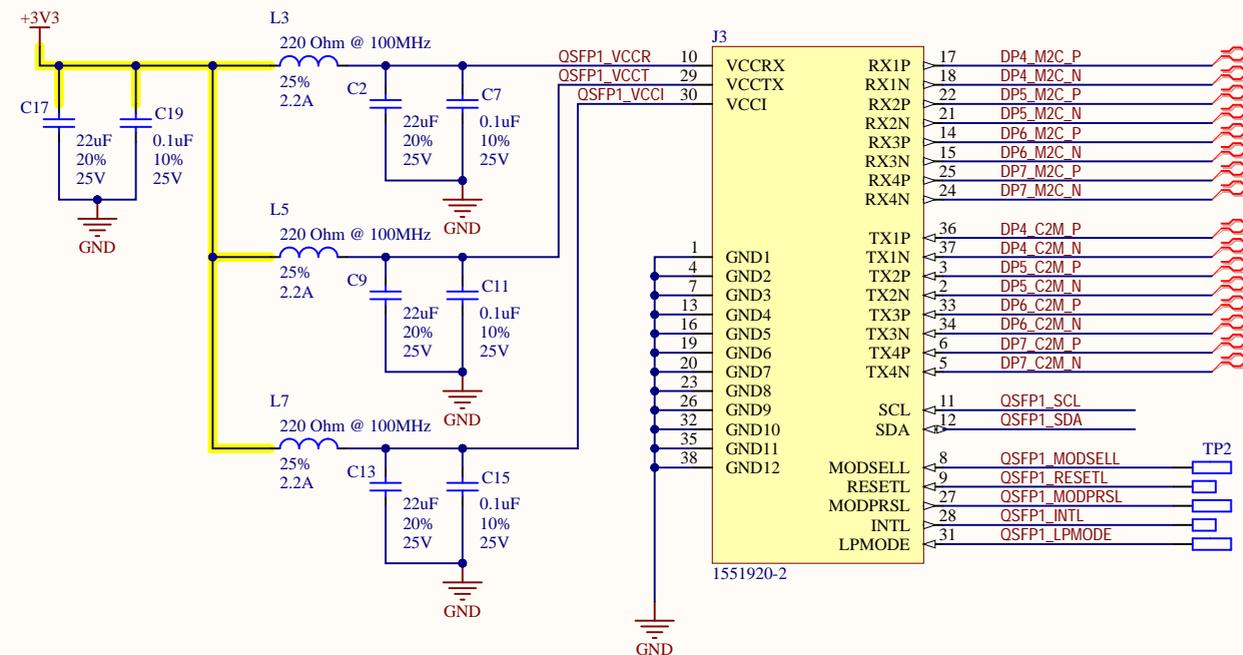
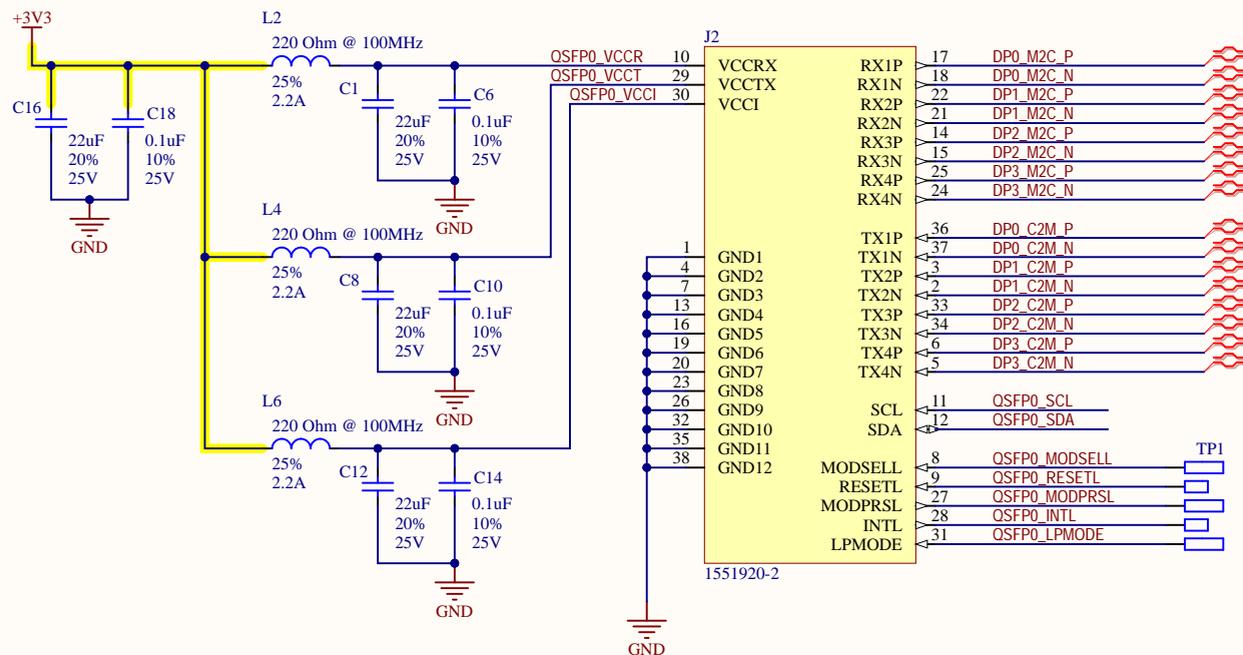
**opsero**  
ELECTRONIC DESIGN

TITLE: 2x OSFP28 FMC  
SHEET: Voltage Translation  
CONFIG: Standard

PROJECT: Ethernet FMC	DRAWN: J Johnson	DATE: 2025-02-24
SIZE: B	SCH PIN: OP120-01-SCH.	REV. B-1
		SHEET 3 OF 5

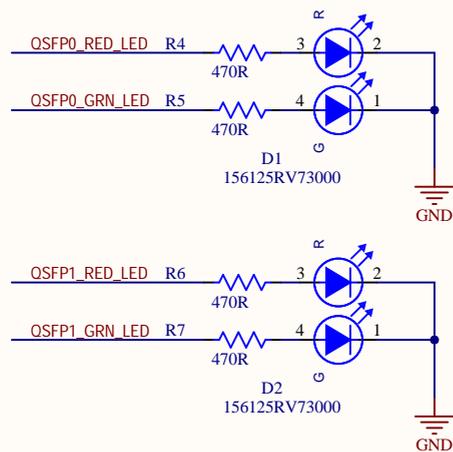
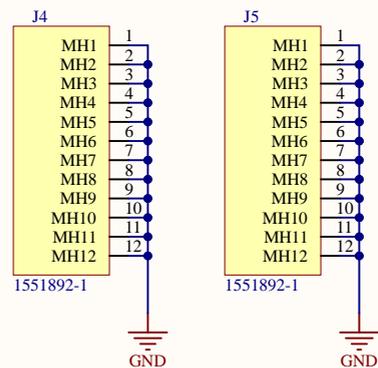
REV.	DESCRIPTION	DATE	APPROVED
B-1	Changed package of I2C translators	2026-02-03	J Johnson

## QSFP28 CONNECTORS

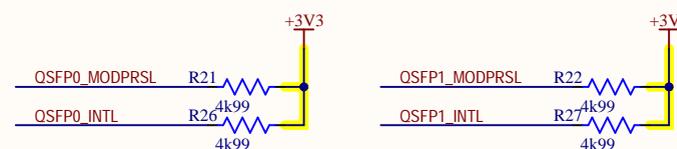


## QSFP LEDS

### QSFP28 CAGES



### QSFP OUTPUT PULL-UPS

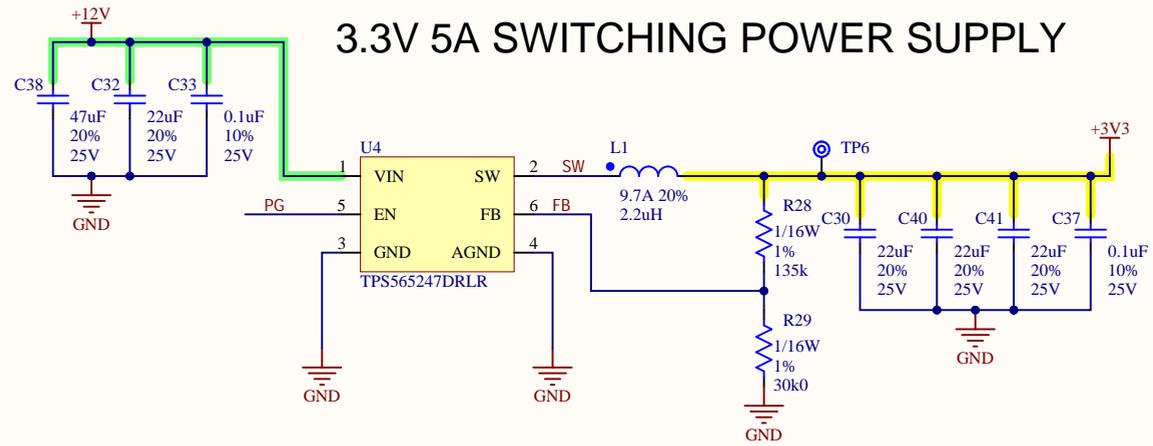


We pull up to 3.3V and then translate to VADJ (rather than just pulling up to VADJ) because some QSFP modules specify a minimum pull-up voltage that is greater than 1.5V (ie. greater than the max VADJ of the Versal boards).

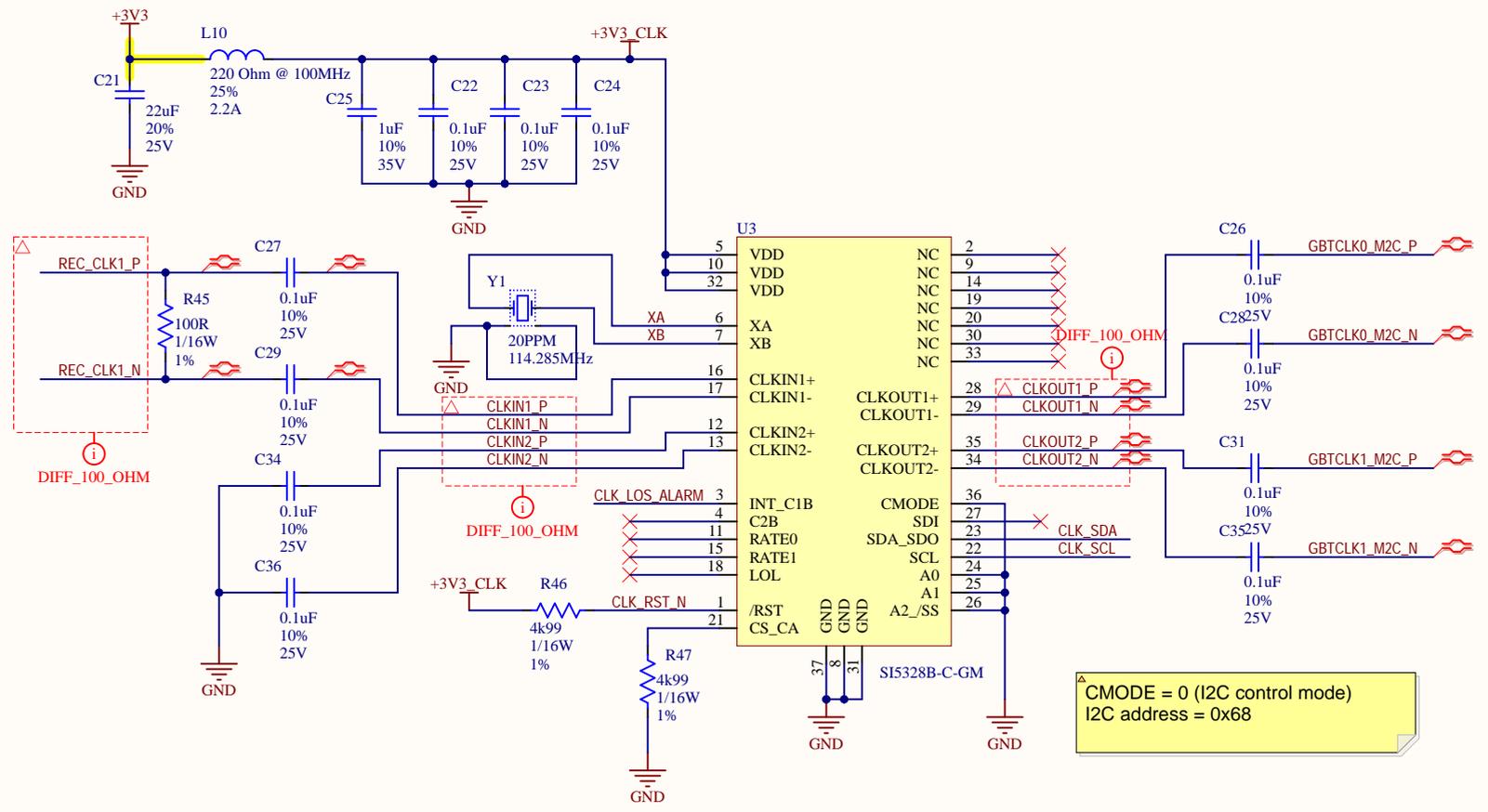
TITLE 2x QSFP28 FMC			
SHEET 2x QSFP28 Cages			
CONFIG. Standard			
PROJECT Ethernet FMC	DRAWN J Johnson	DATE 2025-02-24	
SIZE B	SCH PIN. OP120-01-SCH.	REV. B-1	SHEET OF 4 5

REV.	DESCRIPTION	DATE	APPROVED
B-1	Changed package of I2C translators	2026-02-03	J Johnson

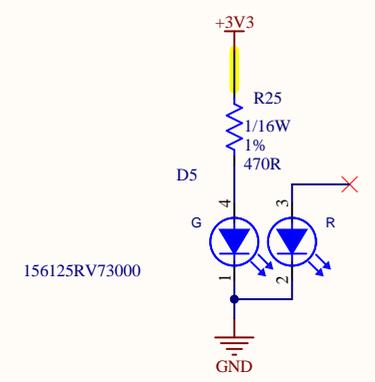
### 3.3V 5A SWITCHING POWER SUPPLY



### JITTER-ATTENUATING CLOCK MULTIPLIER



### POWER GOOD LED



<sup>A</sup> For the POWER GOOD LED to turn ON, the FMC's PG signal must be HIGH and the 3.3V from the buck converter must be active. Failure from either of those will result in this LED being OFF.

<sup>A</sup> CMODE = 0 (I2C control mode)  
I2C address = 0x68

TITLE 2x QSFP28 FMC			
SHEET Power, Clocks and I2C Switch			
CONFIG. Standard			
PROJECT Ethernet FMC	DRAWN J Johnson	DATE 2025-02-24	
SIZE B	SCH PIN. OP120-01-SCH.	REV. B-1	SHEET 5 OF 5